Adaptive, Iterative Closed-Loop Control for the Turn-on of IGBTs with Improved Efficiency

Marius Cenusa,¹ Gabriel Cretu,¹ and Martin Pfost²

¹Robert Bosch Center for Power Electronics, Reutlingen University, Reutlingen, Germany

²Institute of Mechatronics, University of Innsbruck, Austria

Abstract

This paper addresses the turn-on switching process of insulated-gate bipolar transistor (IGBT) modules with anti-parallel free-wheeling diodes (FWD) used in inductive load switching power applications. An increase in efficiency, i.e. decrease in switching losses, calls for a fast switching process of the IGBT, but this commonly implies high values of the reverse-recovery current overshoot. To overcome this undesired behaviour, a solution was proposed which achieves an independent control of the collector current slope and peak reverse-recovery current by applying a gate current that is briefly turned *negative* during the turn-on process. The feasibility of this approach has already been shown, however, a sophisticated control method is required for applying it in applications with varying currents, temperature and device parameters. In this paper a solution based on an adaptive, iterative closed-loop control is proposed. Its effectiveness is demonstrated by experimental results from a 1200 V/200 A IGBT power module for different load currents and reverse-recovery current overshoots.

1 Introduction

Optimizing the switching process of insulated-gate bipolar transistors (IGBTs) is a subject under continuous research, given the wide range of applications in which IGBTs are used. A typical test circuit resembling applications where IGBTs are switching an inductive load is presented in **Figure 1**. Besides an IGBT and the load, a free-wheeling diode (FWD) is required to ensure a path for the load current during the off-state of the IGBT.

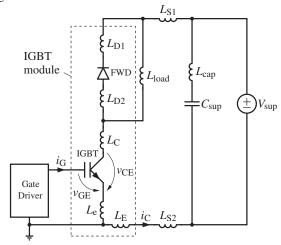


Figure 1 Typical test circuit for an IGBT module switching an inductive load. The module consists of two IGBTs, one high-side and one low-side, each of them having a corresponding FWD in anti-parallel connection. Here, only the low-side IGBT and the high-side FWD are shown because they are of relevance in the switching process considered in this paper. The inductance L_{load} represents the inductive load, the others are parasitic inductances. This paper focuses on the turn-on switching behavior of IGBTs. As demonstrated in [1], the turn-on switching losses can be reduced by fast switching transients. However, if the collector current $i_{\rm C}$ rises very fast (large collector current slope $di_{\rm C}/dt$), high reverse-recovery current overshoots $I_{\rm RR}$ result, which can lead to dynamic avalanche, cf. [2, 3], and destruction of the devices.

Because of this, di_C/dt is generally limited. However, a brief *negative* gate current during IGBT turn-on allows I_{RR} to be chosen independently from the i_C slope. Then, much higher di_C/dt and thus shorter switching times are possible, which can significantly reduce switching losses. This approach [further referred to in this paper as negative gate current (NGC) method] was already presented in [4] and will be briefly recapitulated in Section 2.

However, in order to fully leverage the benefits of the NGC method, a precise control of the gate current is required that also considers changing operating conditions such as varying load currents and temperatures. A solution for this problem is presented in Section 3. This is an important prerequisite for the application of the NGC method in the industry. The effectiveness of the proposed approach is demonstrated experimentally in Section 4, for different load currents and reverse-recovery current overshoots. Finally, in Section 5 the conclusions are drawn.

2 Recapitulation of the Negative Gate Current (NGC) method

Conventionally, the gate driver in **Figure 1** consists of a pulsed voltage source with two voltage levels, on and off, in series with a fixed resistor, to limit the gate current i_G . This leads to a slower increase of the collector current (small

1

value of $di_{\rm C}/dt$), so that $I_{\rm RR}$ can be kept below critical values, see **Figure 2** (a). However, using this approach, further referred to as conventional gate driving (CGD), implies high switching losses, because of the low values of $di_{\rm C}/dt$ and of the collector-emitter voltage slope $dv_{\rm CE}/dt$, see **Figure 2** (a) and (b–dashed line).

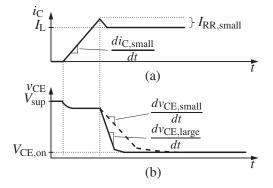


Figure 2 Shown are (a) collector current $i_{\rm C}$ and (b) collector-emitter voltage $v_{\rm CE}$ for the conventional gate driving (CGD) approach (dashed lines) and for the state-of-the-art solutions (solid lines). Note that $i_{\rm C}$ is the same for both methods.

Hence, it has been proposed, e.g. in [5–18], to choose a moderate collector current slope di_C/dt and shorten the turn-on switching process mainly by quickly lowering the collector-emitter voltage v_{CE} after the load current has commuted from the FWD to the IGBT, as in **Figure 2** (solid lines). In these papers, an independent control of di_C/dt and dv_{CE}/dt is achieved, obtaining a low di_C/dt to keep a low I_{RR} , but a high dv_{CE}/dt in order to reduce the switching losses. Nevertheless, the collector current slope di_C/dt and the reverse-recovery current overshoot I_{RR} are still related, preventing the possibility of decreasing the switching losses by increasing di_C/dt .

Contrary to that, an independent control of di_C/dt and I_{RR} is achieved for the first time with the negative gate current (NGC) method which has been presented in [4]. Here, I_{RR} can be kept at moderate values even for high collector current slopes di_C/dt by decreasing the IGBT conductance once the desired I_{RR} is reached. This is done by briefly making the gate current i_G negative, as shown in **Figure 3**. Therefore, the NGC method allows further improvements of the turn-on switching process compared to the state-of-the-art solutions.

3 Adaptive and iterative closed-loop concept for the NGC method

Different control techniques for adjusting the switching transients of IGBTs have been proposed. They can be divided into open-loop and closed-loop controlled gate drives. Since the first approach is not able to satisfactorily compensate the nonlinearities of the IGBT and the variation of the operating point and temperature, a closed-loop solution is required for implementing the NGC method.

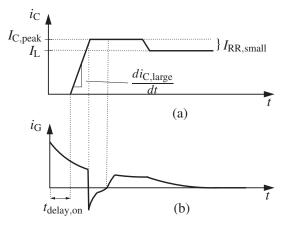


Figure 3 Shown are (a) collector current $i_{\rm C}$ and (b) gate current $i_{\rm G}$ for the negative gate current (NGC) method. The collector current slope used for NGC is larger than the one used in the state-of the-art, see **Figure 2** (a). Still, the value of the overshoot $I_{\rm RR}$ is the same.

The proposed method is intended to be used with very fast transients (so that switching losses can be reduced). In this case, a real-time closed-loop would not be fast enough to react during $i_{\rm C}$ rise. Therefore, the implementation of the NGC method is based on an adaptive, iterative control: Key parameters of the switching transients are measured during a turn-on event. Then, corrections to the driving signals, needed to keep $i_{\rm C}$ as in **Figure 3** (a), are automatically made for the next turn-on. An implementation of the proposed solution is presented in **Figure 4**.

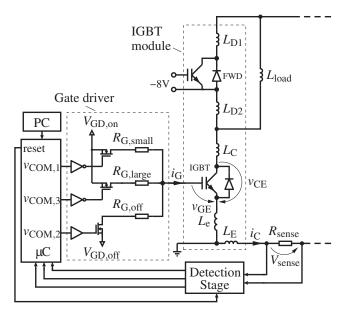


Figure 4 Circuit implementing the negative gate current (NGC) method for the application in **Figure 1**. Here, for simplicity a shunt (R_{sense}) was used to measure i_{C} , but fast inductive current transducers can also be applied.

A detection circuit, which will be described later in Section 3.3, is used to measure the nominal, peak and slope values of $i_{\rm C}$ from a sense resistor $R_{\rm sense}$, after every turn-

2

on. This information is fed into the microcontroller, which uses it to determine the pulse widths of the control signals $v_{\text{COM},1}$, $v_{\text{COM},2}$ and $v_{\text{COM},3}$ for the next turn-on switching of the low-side IGBT.

3.1 Normal operation

During normal operation, the setup works with improved efficiencies compared to the state-of-the-art approaches because of the optimized waveform of the collector current, cf. **Figure 3** (a). It is assumed that this shape has already been obtained for an arbitrary load current. (It will be discussed in Section 3.2 how this can be achieved.) To maintain this optimized waveform and the low overshoot values for slowly changing load currents (which is normal during regular operation), the pulse width of $v_{\text{COM},1}$, denoted as p_1 , see **Figure 5**, is modified accordingly after each turnon. The pulse width of $v_{\text{COM},2}$, denoted as p_2 in **Figure 5**, is kept constant during normal operation.

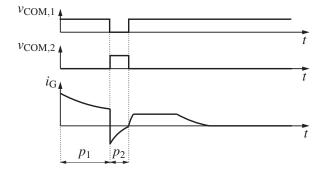


Figure 5 The control signals $v_{\text{COM},1}$ and $v_{\text{COM},2}$, corresponding to $R_{\text{G,small}}$ and $R_{\text{G,off}}$, respectively, used to generate the optimized waveform of i_{G} during normal operation. (Here, $v_{\text{COM},3}$ is not required.)

The length p_1 controls the value of the reverse-recovery current overshoot. It can be defined as the sum of the turnon delay time $t_{delay,on}$, see **Figure 3**, and the time required by the collector current to reach the desired peak value $I_{C,peak}$, i.e. the load current I_L plus the desired overshoot I_{RR} . For a constant collector current slope, p_1 can be expressed as

$$p_1 = t_{\text{delay,on}} + \frac{I_{\text{C,peak}}}{di_{\text{C}}/dt} \,. \tag{1}$$

The value of $t_{\text{delay,on}}$ depends only on $R_{\text{G,small}}$, see **Figure 4**, which means that it stays constant during operation. Therefore, an increase of p_1 leads to a proportional increase of $I_{\text{C,peak}}$. For a specific value of the load current, if the value of p_1 is too high, I_{RR} will also be too high.

The length p_2 determines the duration of the negative gate current. In order to keep the collector current constant once the desired I_{RR} is reached, the conductance of the IGBT must be lowered to a specific value. Therefore, a certain amount of charge must be removed from its gate. This amount is dependent on the values of p_2 and $R_{G,off}$. Given the fact that $R_{G,off}$ is constant during operation, if p_2 is too small, i_C will not have a flat top once it reaches the desired value, but rather it will continue to increase with a smaller slope. This causes an exceedance of the desired I_{RR} . The correction that is applied to the length p_1 after each switching iteration will be calculated as follows. Assuming a constant slope, the variation of the load current from one pulse to another depends linearly on the variation of the rise time of i_C . Since the desired value of the load current for the next switching iteration is generally known (e.g. determined by the motor control), the length of p_1 needed in the next iteration can be predicted from the next and present values of the load current, $I_{L,next}$ and $I_{L,cur}$, respectively, as

$$p_{1,\text{cur}} + \frac{I_{\text{L,next}} - I_{\text{L,cur}}}{di_{\text{C}}/dt} \,. \tag{2}$$

However, it must be noted that the slope of the collector current can vary slightly from one pulse to another, and that small deviations from the desired overshoot may appear if (2) is used. Therefore, a correction needs to be applied to p_1 after each iteration and thus, the next value of p_1 is calculated as

$$p_{1,\text{next}} = p_{1,\text{cur}} + \frac{I_{\text{L,next}} - I_{\text{L,cur}}}{di_{\text{C}}/dt} + \frac{I_{\text{RR,des}} - I_{\text{RR,cur}}}{di_{\text{C}}/dt} , \quad (3)$$

where $I_{\text{RR,cur}}$ represents the current value and $I_{\text{RR,des}}$ is the desired value of the i_{C} overshoot.

3.2 Startup phase

In order to obtain the optimized waveform for the collector current $i_{\rm C}$ needed at the beginning of normal operation, initial values for the lengths p_1 and p_2 , denoted as $p_{1,\text{init}}$ and $p_{2,\text{init}}$, respectively, must be determined. For a given load current, these initial values depend on the temperature, on the parasitic inductances, and on the characteristics of the IGBT. If the latter two parameters are well controlled during fabrication, temperature-dependent initial values can be determined already during the development phase. Otherwise, a startup phase is needed to determine them automatically.

During the startup phase all three control signals $v_{\text{COM},1}$, $v_{\text{COM},2}$ and $v_{\text{COM},3}$ are used, as in **Figure 7**, now also including $v_{\text{COM},3}$, contrary to normal operation. The value of the resistor $R_{\text{G,large}}$ (corresponding to $v_{\text{COM},3}$, see **Figure 4**)

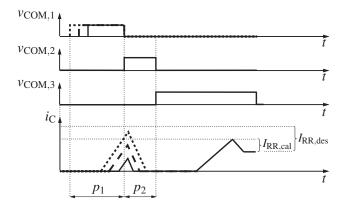


Figure 7 The control signals $v_{\text{COM},1}$, $v_{\text{COM},2}$ and $v_{\text{COM},3}$ used during the startup phase and the collector current i_{C} that they generate. At the end of the startup phase i_{C} will look similar to **Figure 3** (a).

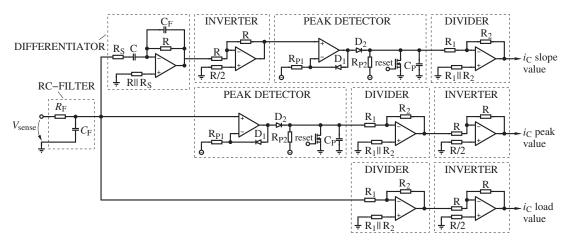


Figure 6 Implementation of detection stage in Figure 4.

is chosen in such a way that $I_{RR,cal}$, the maximum value of the overshoot given by the pulse generated with $v_{COM,3}$, is smaller than the desired value, $I_{RR,des}$ (see **Figure 7**), even for the highest load current. A test pulse is also generated prior to the aforementioned one, using $v_{COM,1}$. It is used only in the startup phase for determining $p_{1,init}$ and $p_{2,init}$ and it does not influence the current through the load during this phase. The two pulses are clearly separated, as to not influence each other, by completely turning off the IGBT after the first one, using $v_{COM,2}$, as shown in **Figure 7**.

 $R_{G,small}$ is chosen small enough to obtain large values for di_C/dt . The initial width of $v_{COM,1}$, i.e. p_1 , is smaller than $t_{delay,on}$ in **Figure 3**, which means that the test pulse will not appear at the very beginning. Then, p_1 is increased in small steps, after each switching iteration, until the overshoot becomes larger than $I_{RR,cal}$, see **Figure 7** (dotted line). In order to determine the initial value for normal operation $p_{1,init}$, the time needed to further increase the peak collector current until it reaches the desired value must be added to the current value of p_1 , denoted as $p_{1,cur}$. Thus, for the same load current, the value of $p_{1,init}$ can now be calculated as

$$p_{1,\text{init}} = p_{1,\text{cur}} + \frac{I_{\text{RR,des}} - I_{\text{RR,cur}}}{di_{\text{C}}/dt} \,. \tag{4}$$

Afterwards, the length p_2 is decreased in small, fixed steps until the overshoot slightly increases over the desired value. p_2 is restored to its previous value, i.e. the smallest value for which $I_{\rm RR}$ is still below $I_{\rm RR,des}$, thus obtaining $p_{2,\rm init}$. With $p_{1,\rm init}$ and $p_{2,\rm init}$ now being known, normal operation as described in Section 3.1 can commence.

3.3 Implementation of the detection stage

In order to implement the closed-loop control concept, the nominal, peak and slope values of the collector current $i_{\rm C}$ must be measured and sent to the microcontroller after each pulse. The detection stage required for this is implemented as shown in **Figure 6**.

The voltage on the sense resistor V_{sense} in **Figure 4** is filtered by a RC-filter in order to cancel the influence of the series parasitic inductance of R_{sense} . Then, the slope is determined by a differentiator, followed by a peak detector, which holds the value of the slope long enough for the microcontroller to read it (upper signal path in **Figure 6**). The

peak value of the current is determined by a peak detector (middle signal path in **Figure 6**), and the value of the load current flowing through the IGBT can be easily read directly on the filtered $i_{\rm C}$ waveform (lower signal path in **Figure 6**). The peak detectors are reset once the microcontroller has read the required information, using a signal generated by the latter. The dividers and inverters are used to adjust the signals to the 3.3 V input of the microcontroller.

4 Experimental results

In order to validate the effectiveness of the proposed closed-loop control method, the testbench in **Figure 4** was used to create a burst of pulses that increase from 50 A to 200 A in steps of 25 A. (This step size is much larger than what is common in typical applications.) The low-side switching device, as well as the high-side FWD were part of a state-of-the-art 1200 V/200 A IGBT power module. Measurement results are shown in **Figure 8**. (For clarity, only every second pulse is plotted.) Initial values for p_1 and p_2 have been automatically determined during startup. It can be seen that, although the pulses vary in amplitude from one iteration to the other, the i_C overshoot I_{RR} is maintained at the desired value, in this case 60 A. The pulses obtained with the CGD at the same I_{RR} have considerably lower slopes, as can be seen in **Figure 8** (dotted lines).

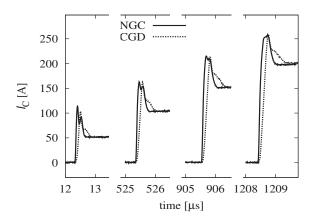


Figure 8 Burst of pulses with increasing amplitudes for NGC (solid lines) and CGD (dotted lines).

The waveforms for the collector current and gate current during normal operation are shown in **Figure 9** for a load current of 125 A and a desired $i_{\rm C}$ overshoot of 60 A. The obtained results are in concordance with the desired implementation of the NGC method, see **Figure 3**. For other values of load currents, $i_{\rm C}$ and $i_{\rm G}$ waveforms look similar.

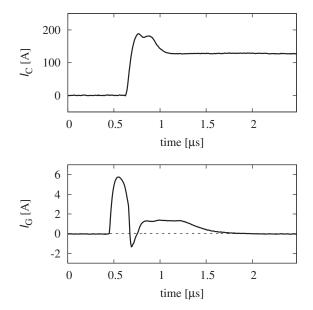


Figure 9 Shown are the collector current $i_{\rm C}$ and the gate current $i_{\rm G}$ for a load current of 125 A during normal operation. These waveforms are obtained for the NGC method and they correspond to the desired waveforms in **Figure 3**.

In order to further demonstrate the efficiency of the proposed method for the 1200 V tested module, the IGBT turn-on switching losses were calculated for both the CGD and the NGC methods for a I_{RR} of 60 A. The results are presented in **Figure 10** for different load currents. They demonstrate the efficiency of the proposed method, achieving improvements in turn-on switching losses up to 48 %. The major advantage of using the NGC method is shown in **Figure 11**. Here, the improvements obtained with the

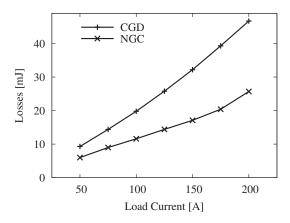


Figure 10 Comparison of the IGBT turn-on switching losses of the CGD and the NGC for a I_{RR} of 60 A, plotted over the load current. The symbols correspond to the measurements, the lines are guides for the eye.

proposed method over CGDs are analyzed separately during the rise of the collector current and during the fall of the collector-emitter voltage, respectively, for a I_{RR} of 60 A. The state-of-the-art solutions obtain improvements over CGDs only during the fall of v_{CE} , as can be seen in **Figure 2**. In addition to that, **Figure 11** shows that the NGC method obtains significant improvements also during the rise of i_{C} , leading to highly increased efficiencies, even with respect to the state-of-the-art methods.

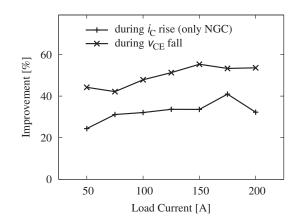


Figure 11 Shown are the improvements in turn-on switching losses of the NGC method over CGDs during the rise of the collector current $i_{\rm C}$ and during the fall of the collector-emitter voltage $v_{\rm CE}$, respectively, for a collector current overshoot $I_{\rm RR}$ of 60 A, plotted over the load current. The symbols correspond to the measurements, the lines are guides for the eye.

The efficiency of the proposed automatically controlled method was also experimentally verified for different values of the overshoot I_{RR} . Figure 12 shows that considerable improvements are obtained even for higher values of I_{RR} . Larger improvements are observed for lower values of I_{RR} , which is also when the stress on the devices imposed by the reverse-recovery current overshoot is lower.

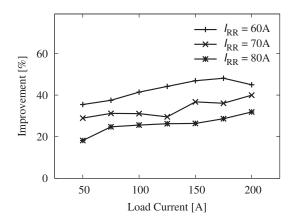


Figure 12 Shown are the improvements in turn-on switching losses of the NGC method over CGD for different reverse-recovery current overshoots I_{RR} , plotted over the load current. The symbols correspond to the measurements, the lines are guides for the eye.

5 Conclusion

An improved method for controlling the turn-on switching process of IGBT power modules was implemented using an adaptive, iterative closed-loop control. This implies measuring the switching transients during one switching event and automatically making corrections to the driving signals for the next event, in order to have an optimized waveform for the collector current. The algorithm needed to implement the proposed solution contains only simple calculations, based on information from the previous pulse. These are measured using a straightforward detection circuitry that could even be integrated in an IC, which makes the proposed solution easy to implement.

The functionality of the proposed closed-loop control has been experimentally demonstrated for load currents that vary from one switching iteration to another. The high di_C/dt achievable with the proposed solution allows considerable reduction of turn-on switching losses. Thus, improvements up to 48% have been experimentally demonstrated for a 1200 V/200 A power module at different load currents. At the same time, a moderate value for the reverse-recovery current overshoot of 60 A was maintained during the entire operation, i.e. for a multitude of load currents. This reduces the stress on the components, opening up possibilities for selection of components with lower losses, e.g. faster FWDs.

6 Literature

- L. Chen and F. Z. Peng, "Switching loss analysis of closed-loop gate drive," in *Proc. of the 25th Annu. IEEE Applied Power Electron. Conf. and Expo.* (*APEC*), Palm Springs, CA, USA, Feb. 2010, pp. 1119–1123.
- [2] A. Porst, "Ultimate limits of an IGBT (MCT) for high voltage applications in conjunction with a diode," in *Proc. of the 6th IEEE Int. Symp. Power Semicond. De*vices and ICs (ISPSD), Davos, Switzerland, May-Jun. 1994, pp. 163–170.
- [3] M. T. Rahimo and N. Y. A. Shammas, "Freewheeling diode reverse-recovery failure modes in IGBT applications," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 661–670, Mar.-Apr. 2001.
- [4] M. Cenusa, G. Cretu, and M. Pfost, "An improved method of controlling IGBT modules using an optimized gate current waveform," in *Proc. of the 8th Int. Conf. on Integrated Power Systems (CIPS)*. Nuremberg, Germany: VDE, Feb. 2014, pp. 1–6.
- [5] A. Galluzzo, M. Melito, G. Belverde, S. Musumeci, A. Raciti, and A. Testa, "Switching characteristic improvement of modern gate controlled devices," in *Proc. of the 5th European Conf. on Power Electron. and Appl. (EPE)*, Brighton, UK, Sep. 1993, pp. 374– 379 vol.2.
- [6] S. Musumeci, A. Raciti, A. Testa, A. Galluzzo, and M. Melito, "A new adaptive driving technique for high current gate controlled devices," in *Proc. of the*

9th Annu. IEEE Applied Power Electron. Conf. and Expo. (APEC), Orlando, FL, USA, Feb. 1994, pp. 480–486 vol.1.

- [7] C. Licitra, S. Musumeci, A. Raciti, A. Galluzzo, R. Letor, and M. Melito, "A new driving circuit for IGBT devices," *IEEE Trans. Power Electron.*, vol. 10, no. 3, pp. 373–378, May 1995.
- [8] A. Consoli, S. Musumeci, G. Oriti, and A. Testa, "An innovative EMI reduction design technique in power converters," *IEEE Trans. Electromagn. Compat.*, vol. 38, no. 4, pp. 567–575, Nov. 1996.
- [9] S. Musumeci, A. Raciti, A. Testa, A. Galluzzo, and M. Melito, "Switching-behavior improvement of insulated gate-controlled devices," *IEEE Trans. Power Electron.*, vol. 12, no. 4, pp. 645–653, Jul. 1997.
- [10] S. Park and T. M. Jahns, "Flexible dv/dt and di/dt control method for insulated gate power switches," *IEEE Trans. Ind. Appl.*, vol. 39, no. 3, pp. 657–664, May-Jun. 2003.
- [11] V. John, B. Suh, and T. Lipo, "High-performance active gate drive for high-power IGBTs," *IEEE Trans. Ind. Appl.*, vol. 35, no. 5, pp. 1108–1117, Sep.-Oct. 1999.
- [12] Z. Wang, X. Shi, Y. Xue, L. M. Tolbert, and B. J. Blalock, "A gate drive circuit of high power IG-BTs for improved turn-on characteristics under hard switching conditions," in *IEEE 13th Workshop on Control and Modeling for Power Electron. (COM-PEL)*, Kyoto, Japan, Jun. 2012, pp. 1–7.
- [13] G. Schmitt, R. Kennel, and J. Holtz, "Voltage gradient limitation of IGBTs by optimised gate-current profiles," in *Proc. of the 39th Annu. IEEE Power Electron. Specialists Conf. (PESC)*, Rhodes, Greece, Jun. 2008, pp. 3592–3596.
- [14] P. J. Grbovic, "An IGBT gate driver for feed-forward control of turn-on losses and reverse recovery current," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 643–652, Mar. 2008.
- [15] N. Idir, R. Bausiere, and J. J. Franchaud, "Active gate voltage control of turn-on di/dt and turn-off dv/dt in insulated gate transistors," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 849–855, Jul. 2006.
- [16] H. Lee, Y. Lee, B. Suh, and D. Hyun, "An improved control scheme for snubberless operation of high power IGBTs," in *Proc. of the 32nd IEEE Ind. Appl. Soc. Annu. Meet. (IAS)*, vol. 2, New Orleans, LA, USA, Oct. 1997, pp. 975–982 vol.2.
- [17] L. Dang, H. Kuhn, and A. Mertens, "Digital adaptive driving strategies for high-voltage IGBTs," in *Proc.* of the 3rd IEEE Energy Convers. Congr. and Expo. (ECCE), Phoenix, AZ, USA, Sep. 2011, pp. 2993– 2999.
- [18] Y. Lobsiger and J. W. Kolar, "Closed-loop IGBT gate drive featuring highly dynamic di/dt and dv/dt control," in *Proc. of the 4th IEEE Energy Convers. Congr. and Expo. (ECCE)*, Raleigh, NC, USA, Sep. 2012, pp. 4754–4761.