

Energy Capability of SiC MOSFETs

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Abstract—The superior electrical and thermal properties of silicon carbide (SiC) allow further shrinking of the active area of future power semiconductor devices. A lower boundary of the die size can be obtained from the thermal impedance required to withstand the high power dissipation during a short-circuit event. However, this implies that the power distribution is homogeneous and that no current filamentation has to be considered. Therefore, this work investigates this assumption by evaluating the stability of a SiC-MOSFET over a wide range of operation conditions by measurements up to destruction, thermal simulations, and high-temperature characterization.

I. INTRODUCTION

Based on the high thermal conductivity of silicon carbide, the SiC-MOSFET is expected to excel in applications with high power dissipation. Therefore, the short-circuit behavior has been investigated in previous papers, e.g. [1], [2]. In this context, hot-spot formation has been considered as aggravating factor, see [3]. However, this assumption does not agree with the very high energy capability often observed. Contrary to the electro-thermal stability of silicon power MOSFETs, which has been studied extensively in [4] and [5], little is known about the characteristics of SiC-MOSFETs at elevated temperatures. Additionally, there appears to be a multitude of potential failure mechanisms, including the activation of the parasitic NPN transistor [6], the degradation of the MOS system [7], and melting of the top metalization [8], [9]. The purpose of this paper is to present a thorough electro-thermal characterization of a commercially available 650 V 120 mΩ SiC MOSFET up to 538 °C, including measurements up to destruction and three-dimensional electro-thermal simulations.

The paper is structured as follows. In Sec. II, the short-circuit behavior is reviewed by measurements covering the whole nominal range of the device. In Sec. III, the device characterization is extended up to very high temperatures to extract the temperature-dependent threshold voltage V_{TH} . In Sec. IV, measurements and numerical simulations are used to investigate the failure mechanism.

II. SHORT-CIRCUIT MEASUREMENTS

In the first measurement, the short-circuit behavior is analyzed for a packaged device and therefore limited to temperatures from -50 °C to 175 °C. The results displayed in Fig. 1 indicate stable behavior for high V_{GS} since $\partial I_D / \partial T$ is negative and unstable behavior for low V_{GS} where $\partial I_D / \partial T$ is positive, cf. [10]. For intermediate values of V_{GS} , intersections of I_D can be observed as the device heats up during the pulse. This behavior implies the existence of a temperature compensation point (TCP), which is confirmed by the transfer

characteristics extracted from the short-circuit measurements, see Fig. 2. Here, a reduced V_{DS} of 100 V was used, which keeps the transistor biased in the saturation region but limits self-heating. However, contrary to common Si-MOSFETs, the TCP is located very close to the maximum rated V_{GS} voltage.

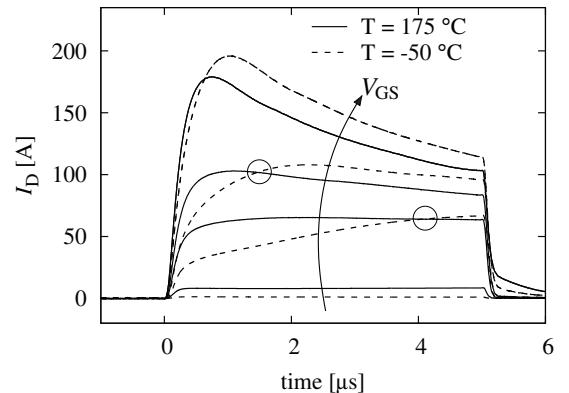


Fig. 1. Drain currents measured for typical short-circuit pulses for $V_{DS} = 600$ V and $V_{GS} = 7$ V, 13 V, 16 V, 22 V. While I_D curves for -50 °C and 175 °C run in parallel for $V_{GS} = 22$ V and $V_{GS} = 7$ V, intersections (marked by circles) can be observed for $V_{GS} = 13$ V and $V_{GS} = 16$ V.

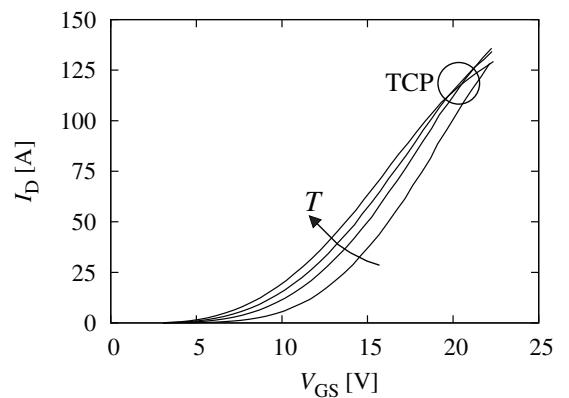


Fig. 2. The transfer characteristics at $V_{DS} = 100$ V as extracted from the short-circuit measurements at moderate ambient temperatures of -50, 25, 100, 175 °C.

III. HIGH-TEMPERATURE CHARACTERIZATION

To evaluate the stability of the device at high temperatures, the transfer characteristics are measured using a specialized setup, see [11], also Fig. 3. In this work, the bare die is sintered into a ceramic package and connected via gold bonds to the

leadframe. A drop of silver-sinter paste is used as separation layer to prevent the formation of gold-aluminum intermetallics which are known to cause connection problems between the top metalization and the bond wires above 400 °C.

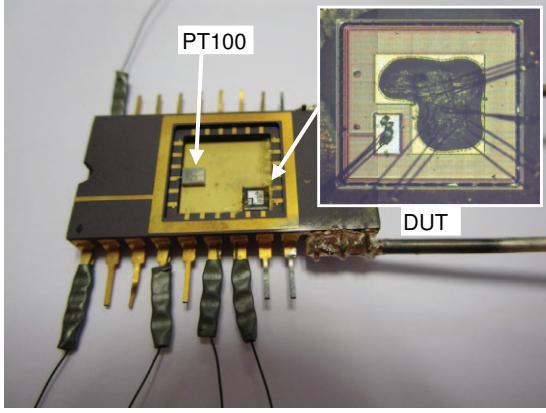


Fig. 3. Mounting used for very-high-temperature measurements. The DUT is sintered to a ceramic package and measured in N_2 atmosphere to avoid oxidation. The actual temperature is verified by a PT100 element mounted close to the DUT.

For the characterization, the device is subjected to high drain-source voltages to ensure operation within the saturation region. The resulting high power dissipation causes significant self-heating. Therefore, very short pulses are required to limit self-heating to a minimum, which in turn complicates the measurement as transient trapping effects move into focus. These effects cause an offset in the drain current, which decays with time [12], [13] and is dependent on the off-state gate voltage $V_{GS,off}$, cf. Fig. 4. The $V_{GS,off}$ dependency can be explained by the additional occupation of interface states in accumulation [14]. The characterization measurements are, therefore, performed for $V_{GS,off} = 0$ V where the least amount of transient behavior is present.

The transfer characteristics measured over a wide temperature range are shown in Fig. 5. The temperature-dependent shift towards lower V_{GS} observed in the transfer characteristics complies with MOS theory below the TCP, cf. [10]. However, the saturation effect at elevated temperatures can not be explained by the mostly linear temperature dependency of V_{TH} known from silicon devices.

Extraction of V_{TH} is performed via the constant current method. This method, although simple, is sufficient in this case since more accurate values are difficult to obtain because of the transient trapping phenomenon mentioned before. The results are displayed in Fig. 6. Linear regression gives a temperature coefficient of -9.4 mV/K for low temperatures and -2.0 mV/K for high temperatures.

A strong temperature dependency of V_{TH} for low temperatures is common in SiC-MOSFETs and can be explained by the very high density of states located at the SiC-SiO₂ interface [15], [16]. The distribution of the interface states within the bandgap has been reported to increase exponentially towards the conduction band edge. With increasing temperature, less

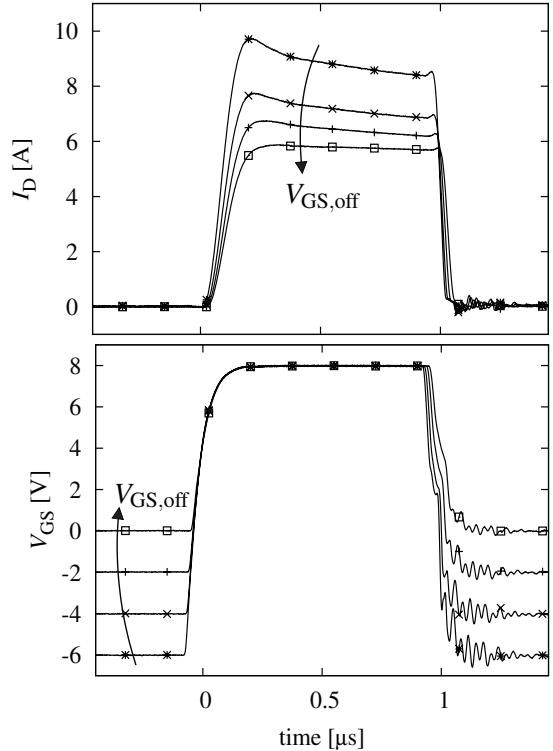


Fig. 4. Typical pulse shapes for $V_{DS} = 200$ V at room temperature. An increase in I_D plus a decay can be observed with decreasing $V_{GS,off}$ values.

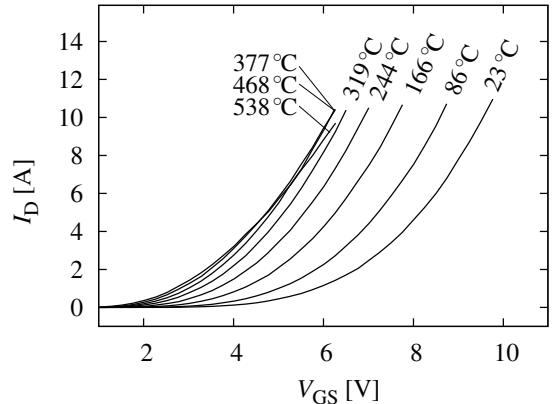


Fig. 5. Transfer characteristics for $V_{DS} = 200$ V and temperatures ranging from 23 °C to 538 °C. Note that values above 400 °C are difficult to distinguish. The traces for 376 °C and 468 °C overlap almost completely, while the trace for 538 °C shows a intersection with the latter two.

interface states are occupied [17]. Therefore, the fraction of V_{GS} necessary to supply for the interface charge also decreases with temperature. This results in a higher inversion charge for a given gate voltage which ultimately appears as a reduction of the V_{TH} dependency with temperature.

The temperature coefficient of -2.0 mV/K observed for high temperatures is in good agreement with the ideal value of -2.48 mV/K calculated by [15], assuming a typical SiC based MOS system without the influence of interface states. This effect could allow for stable operation at high temperatures

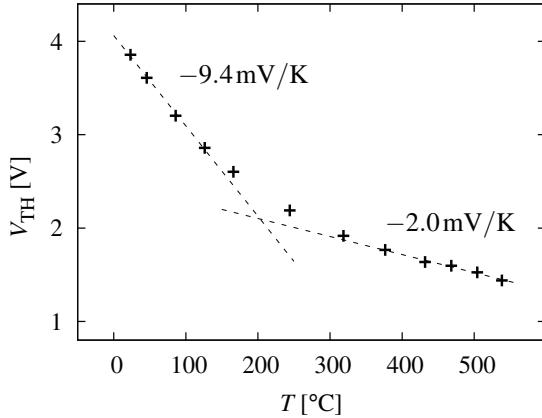


Fig. 6. Threshold voltage V_{TH} over temperature and linear approximation for two regions with different temperature gradients.

where the I_D increase caused by the V_{TH} -shift can be compensated by the reduced carrier mobility, as can be seen from the I_D curves for 377 °C, 468 °C and 538 °C in Fig. 5.

IV. DESTRUCTIVE MEASUREMENTS

To obtain additional information about the stability during rapid self-heating, destructive measurements are carried out. Post-defect optical inspection and electro-thermal temperature simulations based on the approach of [4] are used to identify and explain the failure mechanisms. During the measurements, the devices are operated with constant current by a simple gate control circuit. This technique is advantageous, because V_{DS} and I_D are truly constant. Only V_{GS} changes as the device heats up. Hence, the measurement data can be compared directly to the data obtained by the high temperature characterization.

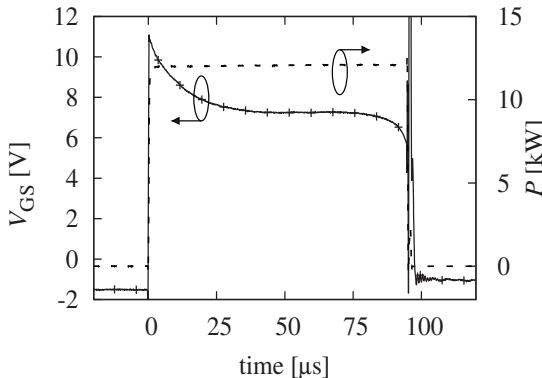


Fig. 7. Destructive measurement for a power dissipation of 12 kW ($V_{DS}=600 \text{ V}$, $I_D=20 \text{ A}$).

A range of devices were subjected to power pulses of 0.6 - 18 kW with increasing pulse widths until breakdown occurred. The observed destruction energies show little variation and range from 0.9-1.5 J. Typical results for a high power pulse of 12 kW are shown in Fig. 7. Here, V_{TH} and therefore V_{GS} undergo very little change from 30 μs to 75 μs, even though the temperature rises drastically during that time span.

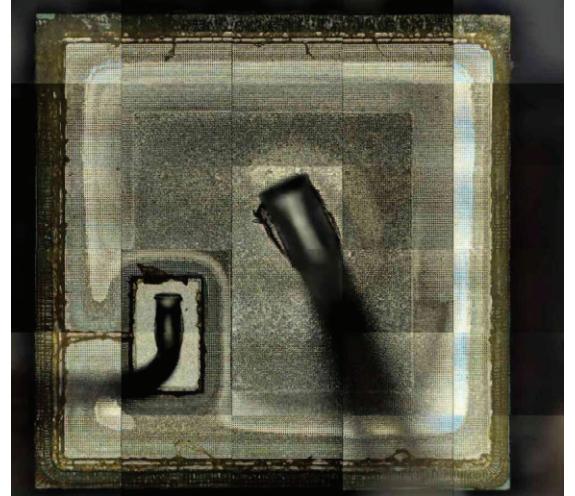


Fig. 8. Device subjected to a 100 μs pulse with $E_{pulse} = 1.08 \text{ J}$, showing uniformly molten top metalization, indicating a homogeneous temperature distribution during heating.



Fig. 9. Device now subjected to a pulse with $I_D=3 \text{ A}$, much lower than in Fig. 8. V_{ps} was 600 V in both cases. Here, the time to destruction is much longer (760 μs instead of 100 μs as for Fig. 8). A burn mark is now observed.

This observation indicates stable electro-thermal behavior, see also I_D in Fig. 5 for temperatures ≥ 377 °C, and explains why the short-circuit robustness is much higher than expected from calculations if only the pronounced V_{TH} -dependency at lower temperatures is considered. For the same reason, current filamentation is not expected at very high temperatures, and uniform heating should be seen. This agrees with observations that the top metalization was molten over the whole active area, see Fig. 8, and not only in a small spot.

However, this is not the case in all operating points, agreeing with [3]. A device subjected to a longer pulse with reduced power exhibits a burn-mark and a smaller, more localized melting of the top metalization, see Fig. 9. The non-uniform temperature distribution accounting for this behavior has been

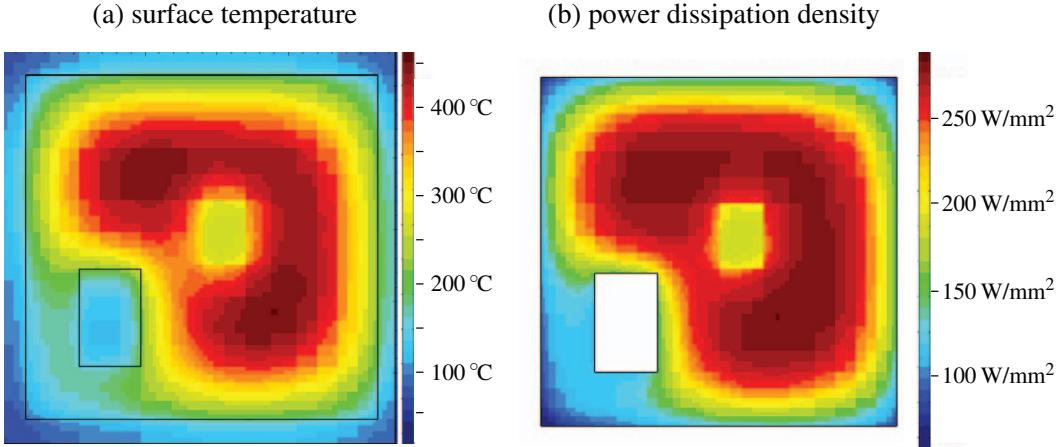


Fig. 10. Numerical 3-D electro-thermal simulation results for (a) surface temperature of the SiC die and (b) the power dissipation for constant $I_D=3$ A and $V_{DS}=600$ V. The plots correspond to 500 μ s heating, destruction is observed after 760 μ s. The position of the burn-mark seen in Fig. 9 agrees with the simulated peak temperature.

confirmed by electro-thermal simulations, see Fig. 10. However, the simulated maximum temperatures are significantly lower than those obtained for Fig. 7. Therefore, the exact mechanism responsible for device failure at lower V_{GS} and thus lower power densities is subject to ongoing research.

V. CONCLUSIONS

An exact understanding of the high temperature characteristics is crucial to determine the short-circuit capabilities and to fully exploit the electro-thermal limits of the SiC MOSFETs. It was found that the very high short-circuit robustness is due to the experimentally observed reduction of $\partial V_{TH}/\partial T$ for temperatures above 350 °C. However, for very low V_{GS} current filamentation is observed, in good agreement with previous work and electro-thermal simulations.

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