Analog Workshop 2017

March 2-3, 2017

Hosted by
Chair of Mixed Signal Circuit Design
Technische Universität Berlin

Organized by
Prof. Dr.-Ing. Friedel Gerfers
Dr.-Ing. Philipp Scholz

Sponsored by

NXP

Inphi
Think fast.

Supported by

VDE ITG CAS

MIXED SIGNAL
MSC
CIRCUIT DESIGN

A Gate Driver IC Based on High-Voltage Energy Storing for GaN Transistors

Achim Seidel, Bernhard Wicht
Robert Bosch Center for Power Electronics
Reutlingen University, 72762 Reutlingen, Germany
Email: {achim.seidel, bernhard.wicht}@reutlingen-university.de

***Abstract*—This work presents a fully integrated GaN gate driver in a 180nm HV BCD technology that utilizes high-voltage energy storing (HVES) in an on-chip resonant LC tank, without the need of any external capacitor. It delivers up to 11nC gate charge at a 5V GaN gate, which exceeds prior art by a factor of 45-83, supporting a broad range of GaN transistor types. The stacked LC tank covers an area of only 1.44mm^2, which corresponds to a superior value of 7.6nC/mm^2.**

In many applications like in renewable energy, electrical cars, and home appliances GaN transistors are utilized to achieve high switching frequencies, shrinking down the size of passives. Also the gate driver circuits are affected by the trend to IC-level integration.

Highly integrated gate drivers still require an external buffer capacitor Cext in the range of 100nF to buffer the drive voltage at turn-on, Fig. 1. In case of fast switching, the effectiveness of Cext is severely reduced, as there is always some parasitic inductance in series.

This drawback can be overcome by integrating the buffer capacitor. Although GaN transistors benefit from 10x smaller gate charge QG compared to silicon, previous designs support only small gate charges in the range of less than 1nC [1]–[3].

The presented fully integrated GaN gate driver [4] (Fig. 1 bottom), comprises a high-voltage energy storing (HVES) circuit, consisting of an LC-tank (LHV, CHV). At driver turn-on, the energy, stored in the high-voltage buffer capacitor CHV discharges resonantly over LHV and the active rectifier and delivers a current pulse with the required gate charge onto GaN gate. The driver has been implemented in a 180nm BCD technology. A gate charge of up to 11nC can be provided, which is 13x more compared to a conventional 5V capacitor with the same layout size and 40% more than the concept in [2].

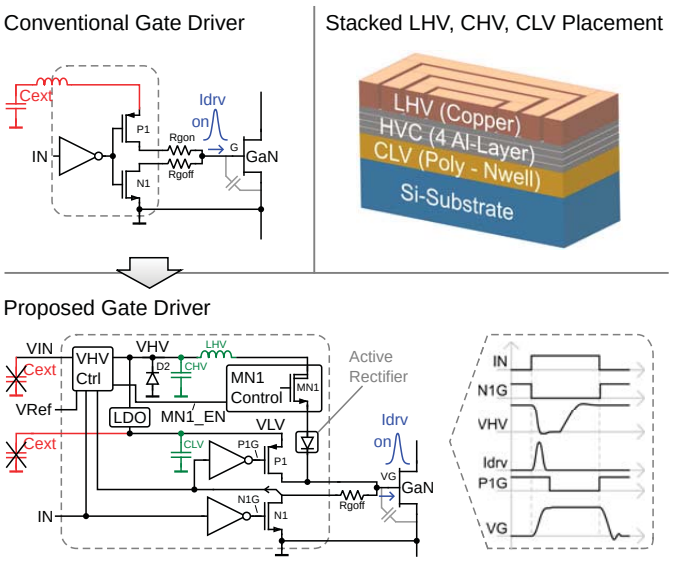

Fig. 1. Conventional gate driver (top left), proposed gate driver (bottom) and inductor / capacitor placement (top right).

References

[1] M. K. Song, L. Chen, J. Sankman, S. Terry, and D. Ma, "16.7 a 20v 8.4w 20mhz four-phase gan dc-dc converter with fully on-chip dual-sr bootstrapped gan fet driver achieving 4ns constant propagation delay and 1ns switching rise time," in *ISSCC Dig. Tech. Papers*, Feb 2015, pp. 1–3.

[2] A. Seidel, M. Costa, J. Joos, and B. Wicht, "Area efficient integrated gate drivers based on high-voltage charge storing," *Solid-State Circuits, IEEE Journal of*, vol. 50, no. 7, pp. 1550–1559, July 2015.

[3] X. Ke, J. Sankman, M. K. Song, P. Forghani, and D. B. Ma, "16.8 a 3-to-40v 10-to-30mhz automotive-use gan driver with active bst balancing and vsw dual-edge dead-time modulation achieving 8.33.4ns constant propagation delay," in *ISSCC Dig. Tech. Papers*, Jan 2016, pp. 302–304.

[4] A. Seidel and B. Wicht, "A 1.3a gate driver for gan with fully integrated gate charge buffer capacitor delivering 11nc enabled by high-voltage energy storing," in *ISSCC Dig. Tech. Papers*, Feb. 5-9, 2017, in press.