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A Ramped-Gate Voltage Sensing Scheme for Embedded Multilevel Flash in Automotive

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***Abstract*—Multilevel-cell (MLC) flash is commonly deployed in today's high density NAND memories, but low latency and high reliability requirements make it barely used in automotive embedded flash applications. This paper presents a time-domain voltage sensing scheme that applies a dynamic voltage ramp at the cells' control gate (CG) in order to achieve fast and reliable sensing suitable for automotive applications.**

I. Introduction

The rise of Advanced Driver Assistance Systems (ADAS) and the growing trend to autonomous driving vehicles requires increasingly powerful microcontrollers. More functionality and higher complexities result in larger application code that has to be stored internally. Despite extensive research on emerging memory technologies to overcome scaling issues, embedded flash is still the predominant non-volatile memory type used in automotive microcontrollers [1]. MLC operation, like it is commonly deployed in high density NAND flash, could also increase storage capabilities here. However, low random access time and high reliability requirements are very challenging for the design of an automotive embedded MLC flash macro.

II. Sensing Principle

The proposed sensing is based on the time-domain source side voltage sensing scheme introduced by Jefremow et al. [2]. It uses a continuous time voltage comparator flipping its output as soon as the bitline voltage, V_{BL} reaches the set threshold, V_{sense}. This allows to define the trigger time, t_{trig}, as the time a cell current requires to accumulate a charge $Q = V_{sense} C_{BL}$ on the bitline capacitance. By strobing the sense amplifiers' outputs with multiple reference timing signals, $t_{ref,0...n}$, multiple cell states can be distinguished. Figure 1 depicts this concept applied on four different cell states (E, P0, P1, P2), which correspond to two bits per cell. The three required reference timings are obtained by sensing the current of three preprogrammed reference cells.

Instead of one constant control gate voltage, V_{CG}, a highly dynamic linear voltage ramp is applied. This delays the current flow through intermediately programmed cells and stretches the timing difference between the individual cell states. Consequently, the relation between

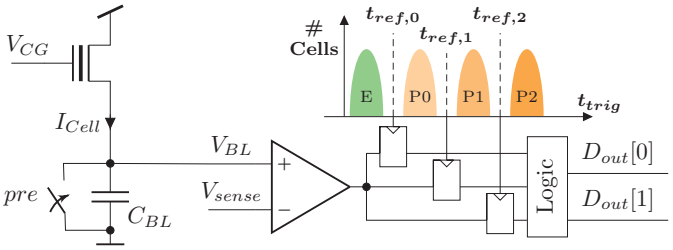

Fig. 1. Simplified schematic of the time-domain voltage sensing applied on a distribution of four cell states (E, P0, P1, P2)

cell threshold level and trigger time gets linearized (see Figure 2), which eases the placement of cell states and makes sensing more robust against threshold variation.

In contrast to common serial sensing schemes used in high density MLC NAND flash applications [3], this ramped-gate biasing allows parallel sensing while still preserving the benefits gained by a variable read voltage. Though driving a voltage ramp to the array's wordlines is clearly complex, the scheme is a good candidate for a fast and reliable embedded MLC flash macro.

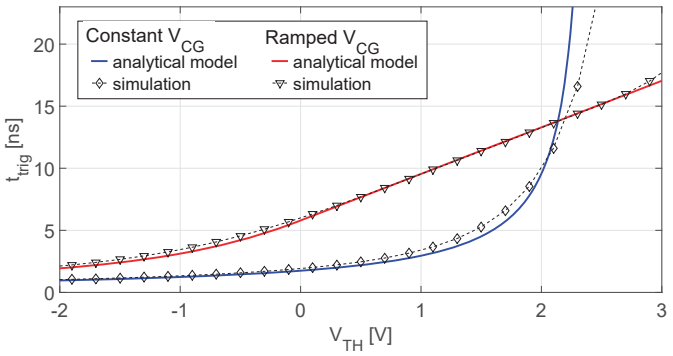

Fig. 2. Transfer characteristic from cell threshold to trigger time obtained by an analytical model and by simulation. Diamonds: constant $V_{CG} = 2.5V$, Triangles: linear voltage ramp starting from $0\ V$ with slope $s = 260\ mV/ns$

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