ASIM-Workshop STS/GMMS 2014

Treffen der ASIM/GI-Fachgruppen:
Simulation technischer Systeme
Grundlagen und Methoden in Modellbildung und Simulation

20. bis 21. Februar 2014 in Reutlingen-Rommelsbach

Tagungsband

Jürgen Scheible (Hrsg.)
Ingrid Bausch-Gall (Hrsg.)
Christina Deatcu (Hrsg.)

Arbeitsgemeinschaft Simulation ASIM in der Gesellschaft für Informatik GI

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Ein Effizienzmodell für getaktete Schaltwandler im Multi–MHz–Bereich

Efficiency Model for Multi-MHz-Converters

Workshop der ASIM/GI-Fachgruppen
20./21. Februar 2014
Achim Seidel
Jürgen Wittmann
Bernhard Wicht

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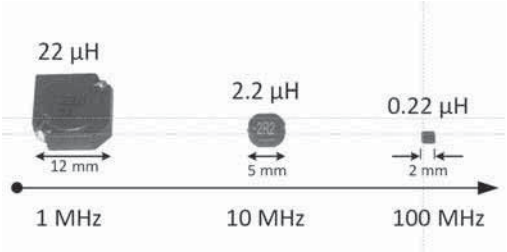
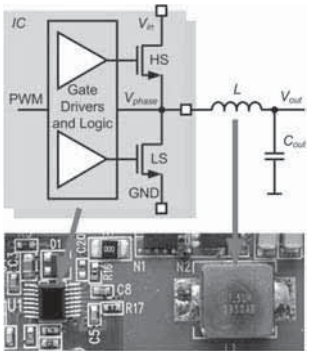
Outline

- Introduction
- Efficiency Model
- Experimental Results
- Analysis with the Efficiency Model
- Conclusion

Cost Reduction by Increasing the Frequency



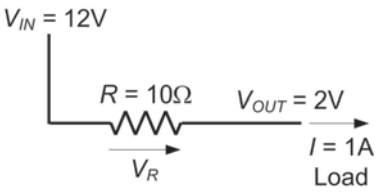


Advantages of smaller devices:

- Less costs, potential for integration
- Better reliability and vibration resistance

How to Convert 12V into 2V?

Using a simple resistor…



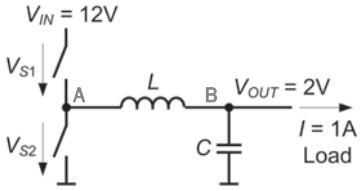
It works, but…

Large power loss at the resistor:

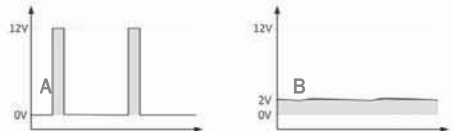
$P_R = V_R \cdot I = 10V \cdot 1A = 10W$
(even larger than P_{out}!)

How to Convert 12V into 2V?

Switched mode conversion…



Pulse-Width Modulation…



Pulse signal Output voltage

It works and has small losses…

Power loss at the switches: $P_S = V_S \cdot I_S$

ideally:
off: $I_S = 0 \rightarrow P_S = 0$
on: $V_S = 0 \rightarrow P_S = 0$

in reality >95% power efficiency possible with frequencies in kHz-range

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Efficiency Model

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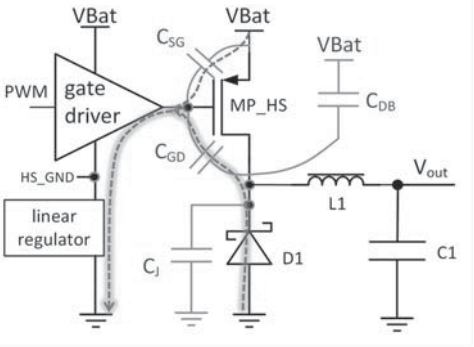
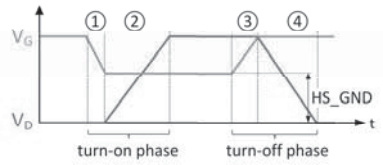
Efficiency Model for Multi-MHz Operation

Example phase ①:





→ Loss cause: C_{GD}
→ Loss location: Schottky diode, linear regulator, gate driver

Determining Losses Including Causes and Locations

		loss cause			
		phase 1	phase 2	phase 3	phase 4
loss location	gate driver Low-Side	C_{GD}, C_{SG}			
	gatedriver High-Side			C_{DG}, C_{SG}	
	linear regulator	C_{GD}, C_{SG}	C_{GD}		
	Schottky diode	C_{GD}			
	FET R_{DSon}		C_{GD}, C_{DB}, C_J		
		transition losses, static losses			

→ Assignment: loss locations and loss causes

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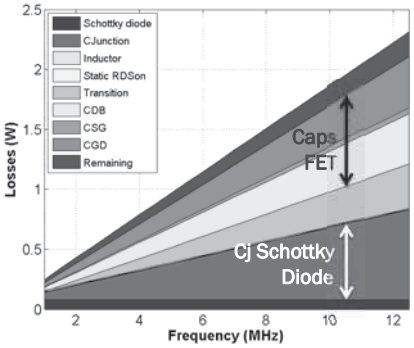
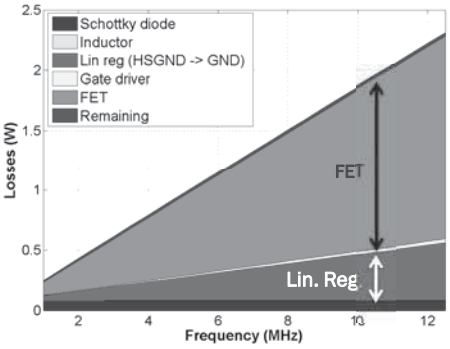
Efficiency Model: Analysis of Losses

Loss causes



Loss locations



Iload = 200 mA
Vin = 40 V

Switching losses dominant at high frequency and high input voltage

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Structure of the Efficiency Model

INPUT
Matlab Script

SIMULATION
Simulink Model

OUTPUT
Matlab Script

- Input arguments
  - Plot settings
  - Converter parameters (i.e. Iout, Vin, Vout, Rdson, Cpar)
- Pre-calculation, i.e.
  - Initial conditions for the transient Simulink model to achieve faster settling
  - Duty cycle

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Structure of the Efficiency Model

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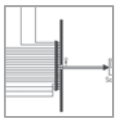

- **Transient Simulink model** with ideal switching transients
- Losses during switching transitions **calculated analytically** based on the transient model results
- Loss results **saved in a variable** for further **post-processing** in a Matlab script

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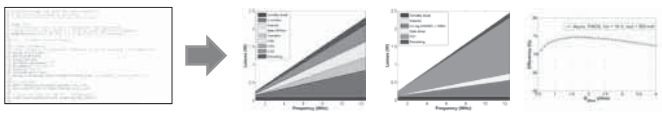
Structure of the Efficiency Model

INPUT
Matlab Script

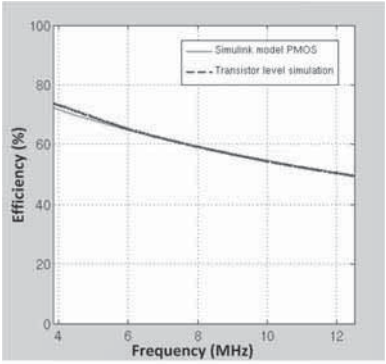
SIMULATION
Simulink Model

OUTPUT
Matlab Script

- In a **Matlab script calculations** and **visualisations** of the Simulink results are done



Verification: Efficiency Model and Transistor Level Simulation



Vin = 18 V
Iload = 200 mA

Deviation beween model and simulation < **2** %

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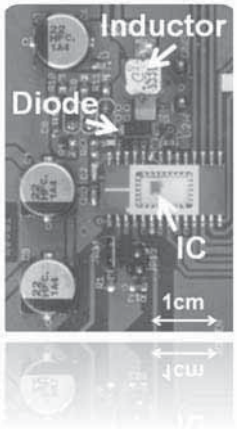
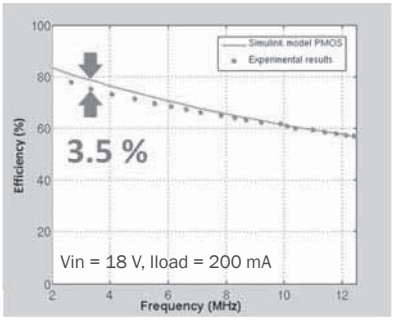
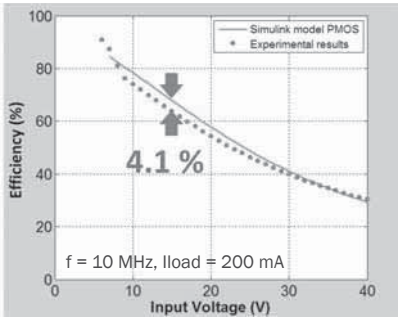
Experimental Results



Experimental Results





- Fully operational @ up to 13 MHz and Vin = 40 V
- Efficiency model verified by experimental results

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Analysis with the Efficiency Model

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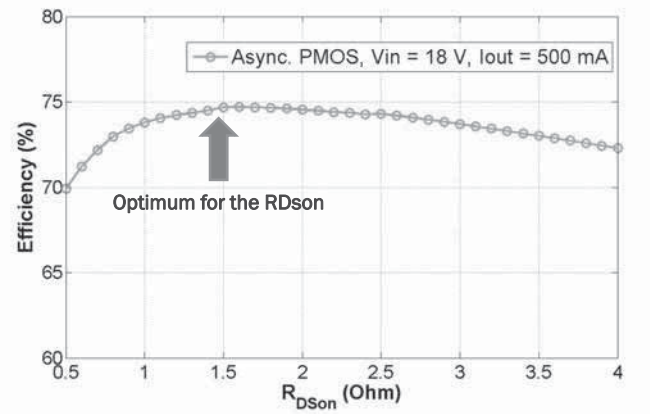
Parameter Optimization of a Given Converter Architecture



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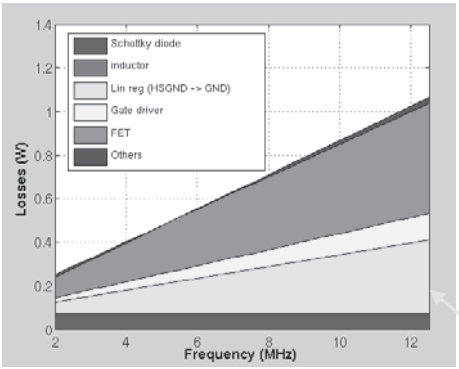
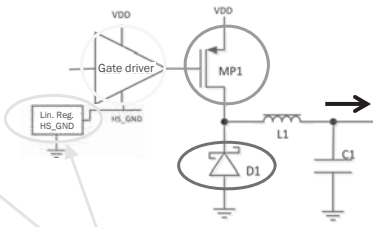
Comparison of Converter Architectures





Vin = 18 V, Iload = 200 mA

Not required with NMOS power FET

→ NMOS typically better than PMOS

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Conclusion

- **MHz converters:**
  - → Reduce system size and cost by faster switching (>10 MHz)
  - → But: power losses increase, precise efficiency model required
  - → Conventional efficiency calculations not suitable anymore
- **The presented efficiency model** allows
  - for dedicated optimization by root cause and loss location
  - an optimization of design parameters
  - to study and compare different converter architectures
- **Measurement results:** Efficiency model matches with less than 3.5 %, main impact from parasitic capacitances

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