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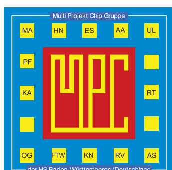

Cooperating Organisation
Solid-State Circuit Society Chapter
IEEE German Section

A Millimeter-Wave Power Amplifier Concept in SiGe BiCMOS Technology for Investigating HBT Physical Limitations

Jonas Wursthorn, Herbert Knapp, Bernhard Wicht

***Abstract*—A millimeter-wave power amplifier concept in an advanced silicon germanium (SiGe) BiCMOS technology is presented. The goal of the concept is to investigate the impact of physical limitations of the used heterojunction bipolar transistors (HBT) on the performance of a 77 GHz power amplifier. High current behavior, collector-base breakdown and transistor saturation can be forced with the presented design. The power amplifier is manufactured in an advanced SiGe BiCMOS technology at Infineon Technologies AG with a maximum transit frequency f_T of around 250 GHz for npn HBT's [1]. The simulation results of the power amplifier show a saturated output power of 16 dBm at a power added efficiency of 13%. The test chip is designed for a supply voltage of 3.3 V and requires a chip size of 1.448 x 0.930 mm².**

***Index Terms*—Millimeter-wave, Power Amplifier, SiGe, BiCMOS.**

I. INTRODUCTION

The demand for vehicle safety is steadily being redefined and tightened by the European New Car Assessment Programme (EURONCAP). Since 2014 it is practically impossible to get a 5-star EURONCAP rating for a new vehicle without an autonomous emergency breaking system (AEB). Automotive manufacturers use frequency modulated continuous wave (FMCW) based radar systems to realize such systems. FMCW radar systems can detect the relative velocity and the distance to the vehicle ahead. These attributes make them also suitable for advanced driver assistance systems like lane change assistants or blind spot detectors. Video and imaging systems might be used additionally to improve the object recognition on the road.

The block diagram of a bi-static (separate transmitter/receiver antenna) FMCW based radar system is shown in Figure 1. A voltage controlled oscillator (VCO) is used as a radio-frequency source that feeds the power amplifier as well as the mixer in the receiver channel. The power amplifier offers a high signal level to the transmitter antenna. The receiver antenna delivers the signal to the mixer input, where it is mixed with the actual local oscillator signal of the VCO. From the time and frequency shift between the two signals the distance and the relative velocity are calculated.

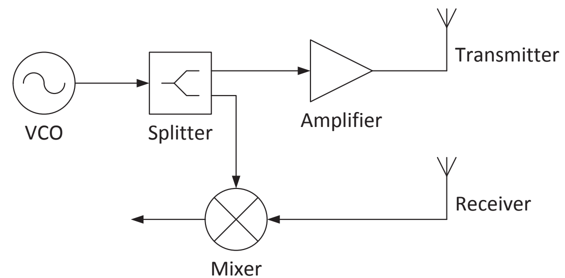

Figure 1: Simplified block diagram of a bi-static FMCW radar system.

In order to detect the reflected signal at the radar module properly, a minimum signal to noise ratio is required. This ratio depends on several parameters but is in the end limited by the power level delivered from the amplifier to the transmitter antenna. The design of the power amplifier is challenging, because physical limitation effects like high current operation or breakdown are often not represented accurately in all transistor models. Measurement results on the power amplifier described in this work are expected to show how an operation close to the physical limits affects its performance, leading to more confident decisions regarding power amplifier design.

The design considerations are described in detail starting with the amplifier topology in Section II. Section III explains how high current effects can be forced with the design. To run the transistors in saturation or breakdown, the bias voltage at the common-base stage can be varied. The bias voltage generation is explained in IV. The implemented test circuit layout is described in Section V. Overall simulation results of the power amplifier can be found in VI. A conclusion is given in Section VII.

II. POWER AMPLIFIER TOPOLOGY

As further automotive circuit designs will be based on the investigations of the designed power amplifier,

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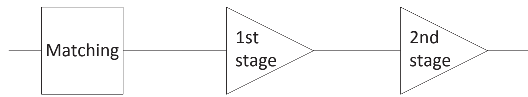

Figure 2: Block diagram of the power amplifier topology.

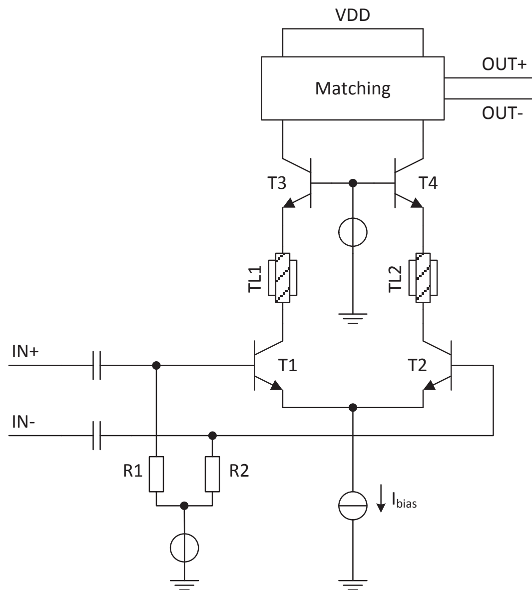

Figure 3: Simplified schematic of the second power amplifier stage.

it has to cover ambient temperatures from -40°C to 125°C. To ensure a preferably constant output power over the temperature range a multi-stage amplifier (2 stages) is chosen wherein the single stages are run in compression mode. This operation mode acts like a buffer if the output power of the previous stage drops due to higher temperature. The gain reduction at high temperatures is mainly caused by the lower current gain and transit frequency in the transistor [2].

In order to have a defined 50 Ω input impedance, a matching network is designed. It consists of a transmission line in series and a capacitance to ground. For the interstage matching between the first and second stage the maximum output power is the main criteria – not a defined impedance level. Therefore the length of the transmission lines between the stages is adjusted. Figure 2 shows a block diagram of the signal path resulting from the mentioned considerations. The matching is realized with transmission lines. The topology of the first and second amplifier stage is similar – the only differences are the device dimensions.

A simplified schematic of the second amplifier stage is shown in Figure 3. The RF signal (IN+/IN-) is fed to a differential common-emitter stage which is DC biased by R1 and R2. A current source I_{bias} at the emitter node is preferred over a resistor for mainly two reasons. On the one hand, the base-emitter diodes of T1 and T2 have a rectifying effect on the applied RF signal, which results in a different DC voltage at the

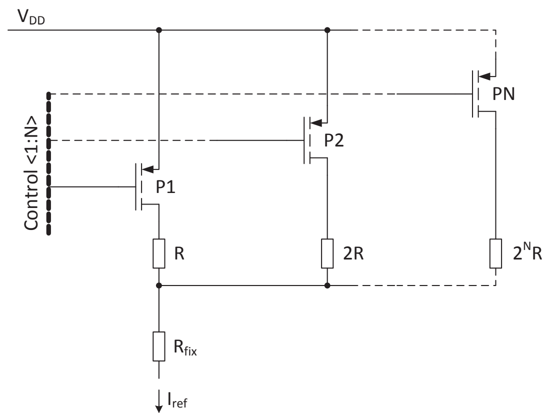

Figure 4: Generation of different reference currents for the current mirror network.

emitters leading to different currents depending on the signal peak when using a resistor. On the other hand the current is limited in case of breakdown when using a current source.

Transmission lines TL1 and TL2 represent the parasitics of the connection between the common-emitter stage (T1/T2) and the common-base stage (T3/T4). The common-base stage offers a low impedance ($1/g_{m3/4}$) to the common-emitter stage. This is essential because otherwise the Miller capacitance between base and collector of T1/T2 would have a huge impact on the amplifiers gain (low pass behavior). The Cascode topology reduces this impact to a minimum as it keeps the collector of T1/T2 practically grounded in terms of RF. For the common-base stage, C_{BC} does not appear between the input and output and is therefore less critical because it does not act as a Miller capacitance.

III. HIGH CURRENT EFFECTS

If a certain limit for the current density in a bipolar transistor is exceeded, the transit frequency is reduced due to the Kirk effect. For a SiGe HBT this effect is shifted to higher frequencies but then f_T drops even faster than for common bipolar transistors [3].

The current density suggested for product design in the used technology is 13 mA/µm². As there is a margin for products, the current density of the considered power amplifier should be increasable to around twice this value. This is realized with a digitally adjustable current mirror. CMOS transistors are switched on/off to increase/decrease the reference current of the current mirror like shown in Figure 4. The design uses $N = 5$ bits to vary the current density from 4 to 25 mA/µm².

High current effects are not represented in the used transistor models so far. Accordingly, there are no simulations showing this effect. For measurements it is expected that the output power will increase with higher currents exceeding the nominal current density. For values far above the suggested current density the

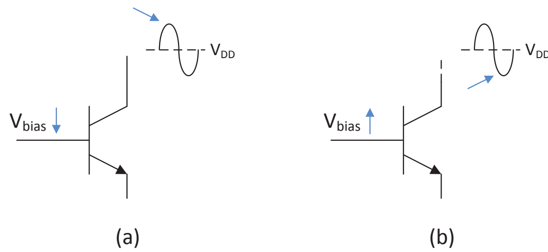

Figure 5: Bias voltage conditions for (a) breakdown and (b) saturation of the used HBT.

output power is expected to drop rapidly due to high current effects in the transistor [2] [3].

IV. Bias Voltage Generation

The region for a useful biasing voltage of the common-base stage is mainly defined by the voltage swing at the collector of the transistor and is nominally between 2 and 2.2 V. If the voltage swing reaches its maximum, the collector-emitter breakdown voltage may be exceeded (see Figure 5(a)) which leads to avalanche multiplication. This effect defines the lower limit of the biasing voltage.

If the output swing is at its minimum, the transistor might enter the saturation region (see Figure 5(b)). This means the base-collector diode will be forward biased, resulting in a malfunction of the power amplifier.

The base bias voltage is generated in a circuit according to Figure 6. The pmosCM_enable bit allows to switch between a PMOS-based and an NMOS-based current mirror. The PMOS-based circuit is used to generate low bias voltages, the NMOS-based part covers the upper voltage range close to V_{DD}. This results in an overlapping bias voltage range from 0.4 to 2.9 V. For measurements it is expected that there is a range within these two voltage limits where the output power is nearly constant.

V. Implemented Test Circuit

The various digital input pins for adjusting the current density or setting the common-base bias voltage are controlled by a serial control interface. The available measurement equipment is only capable of single ended RF signal generation. As the core part of the power amplifier expects a differential signal a balun (balanced-unbalanced) network is required. This network consists of transmission lines and capacitors and is based on the principle described in [4].

A layout of the complete test circuit is shown in Figure 7. Biasing and serial control interface are placed in the left part of the die. The right-hand side contains the RF part with the input pads on the bottom and the differential output pads on the top. Except for

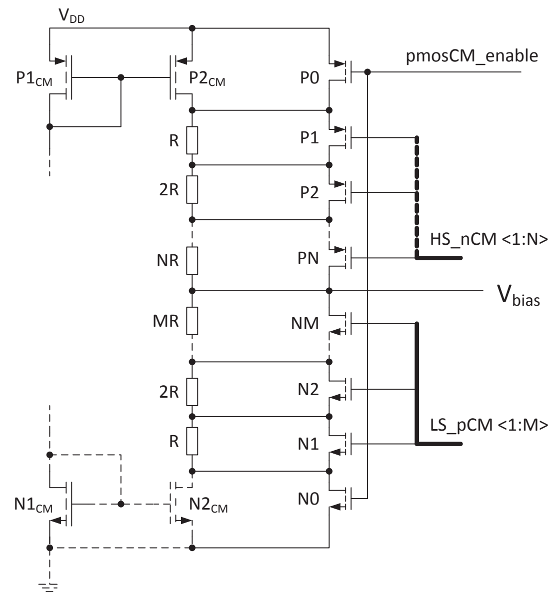

Figure 6: Simplified schematic of the common-base biasing network.

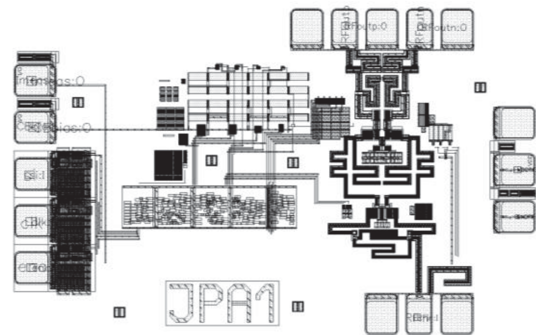

Figure 7: Layout of the implemented test circuit. The RF part is on the right-hand side, biasing and digital part on the left-hand side. The chip size is 1.448 mm x 0.930 mm.

the balun and matching network, the RF layout is highly symmetrical.

VI. Simulation Results

The simulation results of the complete chip for the output power *Pout* and the power added efficiency

$$PAE = \frac{Pout - Pin}{Pdc}$$

are shown in Figure 8 and Figure 9, respectively. A linear gain of ≥25 dB is achieved. The saturated output power is 16 dBm for room temperature. Due to the multi-stage approach the difference in output power (in compression) is less than 1 dBm over the complete temperature range. The PAE simulation also includes the power consumption of the biasing network and the serial control interface and can therefore be further increased for a stand-alone power amplifier. In this configuration the simulation shows a PAE of 13%.

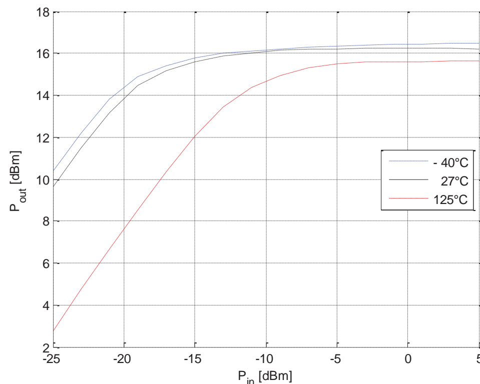

Figure 8: Simulated output power *Pout* vs. input power *Pin* of the complete chip for the automotive temperature range.

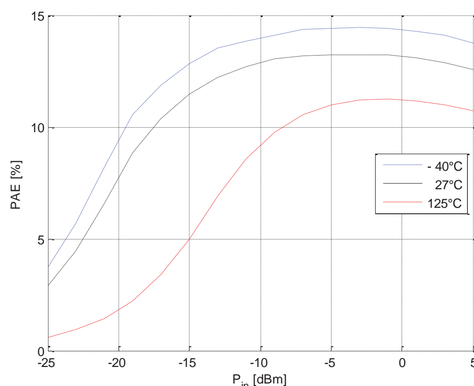

Figure 9: Simulated power added efficiency *PAE* vs. input power *Pin* of the complete chip for the automotive temperature range.

VII. Conclusion

A 77 GHz SiGe BiCMOS power amplifier concept for investigating physical limitations has been presented. The power amplifier simulation shows an output power of 16 dBm with a 13% PAE at 27°C. A serial control interface allows setting the current density in the power amplifier stages and the bias voltage for the common-base stage. The bias voltage can be varied from 0.4 to 2.9 V. The current density can be increased up to 25 mA/µm² to force high current effects.

VIII. Acknowledgement

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