

Machine Learning Assisted Visual Design Space Exploration for GaN Half-Bridges with Output Filter

Philipp Czerwenka¹, Yannick Uhlmann¹, Gernot Schullerus¹

¹ Electronics & Drives, Reutlingen University, Germany

Corresponding author: Philipp Czerwenka, philipp.czerwenka@reutlingen-university.de
 Speaker: Philipp Czerwenka, philipp.czerwenka@reutlingen-university.de

Abstract

This contribution proposes a design space exploration method for GaN half-bridges with output filter, combining analytical and machine learning techniques to achieve a top-down estimate of power loss and system volume. Without explicitly formulating a design strategy, the rapid nature of the method allows designers to approximate an optimal design point or to visualize the causality of different design decisions based on high-level voltage and current system requirements. The presented examples include the estimation of an optimum switching frequency for minimum power loss considering current ripple and the analysis the scaling effect of interleaving parallelization.

1 Introduction

Increasing global electrification demands continuously improving power systems with higher power densities, greater efficiencies, and more sustainable material usage. Such requirements are increasing the design complexity of power electronics systems, necessitating more efficient design procedures. In addition to a growing engineering workforce, automated design methods, which are common in digital and ASIC design, but less so analog and power design, are expected to help meet the growing design demands. This trend is reflected in the growing number of publications on design automation for power electronics since 2005 [1].

Many design automation methods for power electronics proposed in literature focus on optimization techniques [2, 3], see Fig. 1a, and recently include machine learning (ML) approaches [4]. Such methods often require detailed design knowledge or are limited to specific subsystems [5]. Furthermore, designers may hesitate to adopt design automation techniques due to a lack of insight [6]. Simpler and more intuitive automation methods that better reflect the knowledge-based approach of designers are likely to receive a more favorable response. The adoption of design automation techniques in power

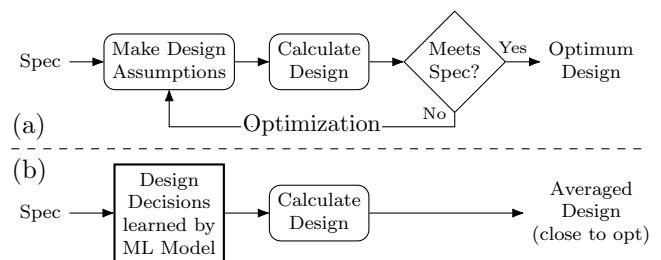


Fig. 1: Comparison of (a) classical optimization-based automated design procedures and the (b) fast exploration strategy proposed in this paper.

electronics is also hindered by the lack of unified component data. Decisions are commonly based on experience and selection processes that are not analytically describable.

In this paper, we propose a novel design space exploration method based on existing knowledge-based analytical relations, extended with machine learning interpolation to address gaps or discrete decision problems. The implemented framework generates near-optimum full system descriptions with component dimensions and enables an analysis for power loss and system volume. The resulting approach is fast, due to the absence of iterations, as shown in Fig. 1b, and modular, facilitating its application to a variety of power electronics systems.

The paper is divided into two parts: Section 2 describes the implementation of our proposed method, detailing the machine learning assisted

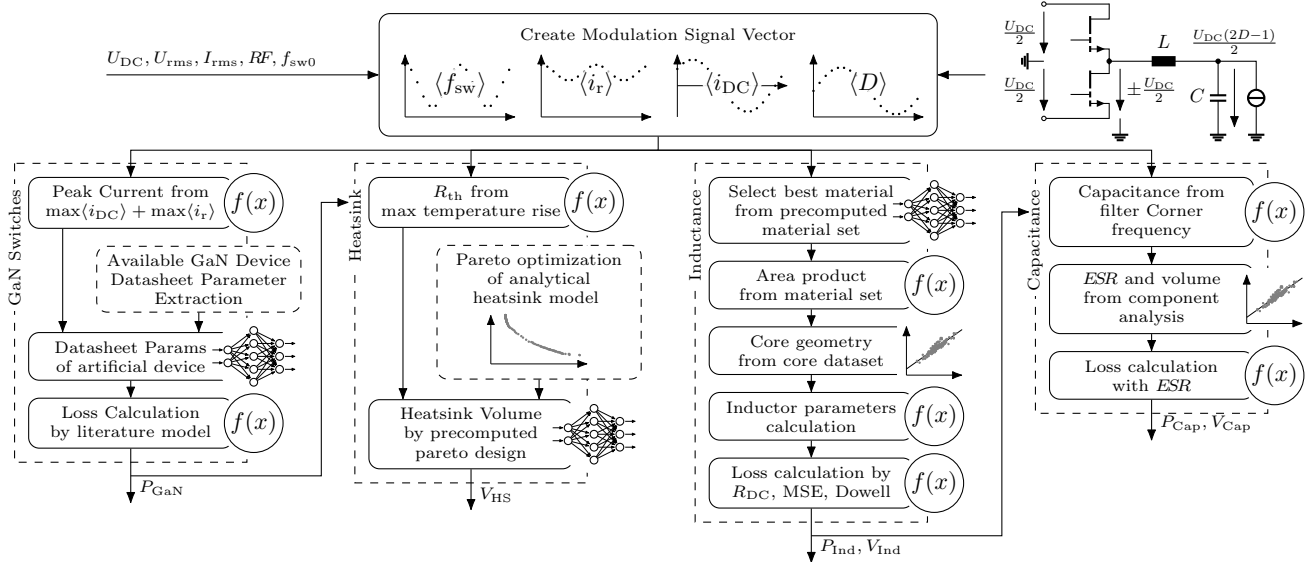


Fig. 2: Flow chart of proposed design exploration method for GaN-based half-bridge with LC output filter, yielding estimated component losses P_c and component volumes V_c for $c \in \{\text{GaN}, \text{HS}, \text{Ind}, \text{Cap}\}$, with system under investigation on the right

power semiconductor modeling (Section 2.1) and associated heatsink design (Section 2.2), as well as the design of power inductors (Section 2.3) and the selection of capacitances (Section 2.4). In Section 3, we present several examples of explored design spaces using our method. Section 4 concludes the paper.

2 Methodology

The core concept of our approach is to use established and proven analytical design and sizing formulas for key components in power electronics design (power stage, inductors, capacitors) and bridge the gaps between them using interpolation and machine learning approaches. Starting from voltage and current requirements in Table 1, we analytically generate discrete time series of frequency $\langle f_{sw} \rangle$, currents $\langle i_r \rangle$ $\langle i_{DC} \rangle$, and duty cycle $\langle D \rangle$. This allows us to capture changing operating points by averaging over one signal period. Using rearranged analytical formulas and interpolation as mentioned above, we calculate component parameters. From these parameters, we determine system performance metrics such as power loss P and volume V , as shown in Fig. 2.

Our combined analytical and machine learning approach is necessary due to the lack of comprehensive data for the entire system. The degrees of freedom are too numerous for practical measurement, and multi-physics domain

Input Parameter	Symbol
DC supply voltage	U_{DC}
Output voltage amplitude	U_{rms}
Output current amplitude (with phase shift)	I_{rms}
Current ripple factor (maximum current to ripple amplitude)	RF
Switching frequency (maximum)	f_{sw0}

Tab. 1: Design inputs for exploration method

simulations are beyond the scope of this publication and typical electronics development design cycles.

Due to the high dimensionality of the parameter space, we do not provide a separate experimental verification of our combination of these methods. Our goal is to demonstrate a proof of concept for automated system design, prioritizing execution speed over accuracy by avoiding iteration. While our approach may not achieve the highest accuracy due to averaging and machine learning errors, it effectively preserves trends and scaling gains for system comparisons, which is our focus.

The novelty of our publication lies in

- the integration of the aforementioned concepts into a unified framework for interdependent execution,
- bridging gaps with custom design relations,
- making quantized decisions continuous by using curve fitting for low-order relations or machine learning-based interpolation for high-order relations.

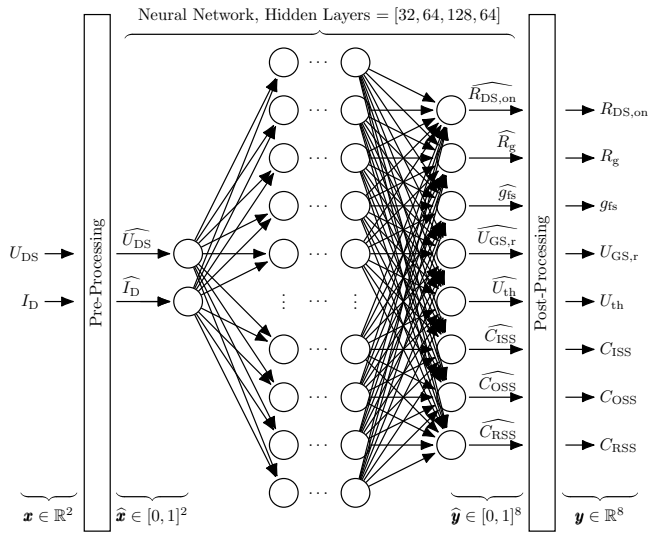


Fig. 3: Multi-layer perceptron used for GaN power device datasheet parameter estimation from voltage and current specification

A description of all design parameters as functions of input voltages and currents is challenging. In the case where no analytical description or datasheet information is available, assumptions are necessary. The following sections will detail the assumptions used in our analyses. Although some assumptions significantly influence the final results, maintaining consistency in the assumptions ensures relative comparability. More detailed modeling of those assumptions in the context of system design remains for further research.

2.1 GaN Switch and Half-Bridge Design

As a power stage we consider a GaN-device based half-bridge circuit (see Fig. 2 top right). Such half-bridges are basic building blocks in power electronics, essential for many topologies of DC-DC converters, grid inverters or motor drive systems. A description of a half-bridge can also be extended to parallelized (e.g. interleaved) or serialized (e.g. multi-level) topologies, as will be discussed in section 3.3.

GaN power devices have recently been brought to market, resulting in a limited total number of different GaN devices. Constructing a continuous design space only considering datasheet parameters of selected device samples is challenging. Therefore, we employ a deep neural network regressor for high-dimensional function approximation and averaging across the available datasheet parameters of GaN power devices. The training is performed such that, given

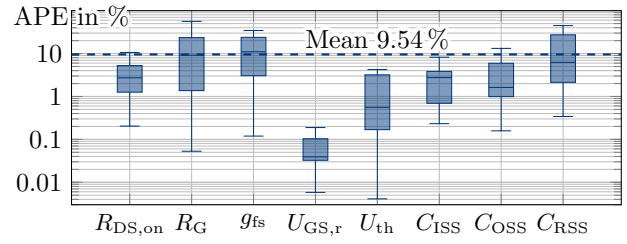


Fig. 4: Absolute percentage error (APE) of GaN power device model parameter prediction

Assumptions	Value
Additional gate resistances $R_{G,on}, R_{G,off}$	10 Ω , 1 Ω
Miller voltage to U_{th} ratio	2.5
Real vs. predicted C_{OSS} ratio	2.5
Device current to peak current ratio	1.8

Tab. 2: Design assumptions for GaN half-bridge

a drain-source voltage U_{DS} and drain current I_D specification, the trained network predicts all necessary device parameters for analytical loss estimation, as illustrated in Fig. 3.

The model error is quantified in Fig. 4 which is comparatively high due to the small sample size of 57 devices. For our purpose, this error is acceptable, as trends are preserved and the goal of creating a continuous design space is achieved. Figure 5 shows selected device parameters as predicted by the ML model.

The analytical loss model in (1) is based on two publications for the switching loss turn-on [7] and turn-off [8] energies, as derived and verified in the respective publications.

$$P_{sw} = \left(\frac{U_{DC} I_D^2}{2g_{fs} \frac{du_{gs}}{dt}} + \sqrt{\frac{Q_{oss}}{g_{fs} \frac{du_{gs}}{dt}}} U_{DC} I_D + \frac{U_{DC}^2 I_D}{6 \frac{du_{gs}}{dt}} + 2C_{oss} U_{DC}^2 \right) f_{sw} \quad (1)$$

For the switching loss, the instantaneous current at each switching event is calculated from $\langle i_{DC} \rangle \pm \langle i_r \rangle$. The gate slew rates $\frac{du_{gs}}{dt}$ are calculated using the resulting RC time constants and gate voltage differences for each section of the switching transient, as defined in the respective publications. The transconductance g_{fs} an average value from the datasheet between V_{th} and $V_{gs,work}$ was extracted, which was also learned by the ML model. The effects of deadtime are not modeled, making our method a best-case approximation regarding reverse conduction loss.

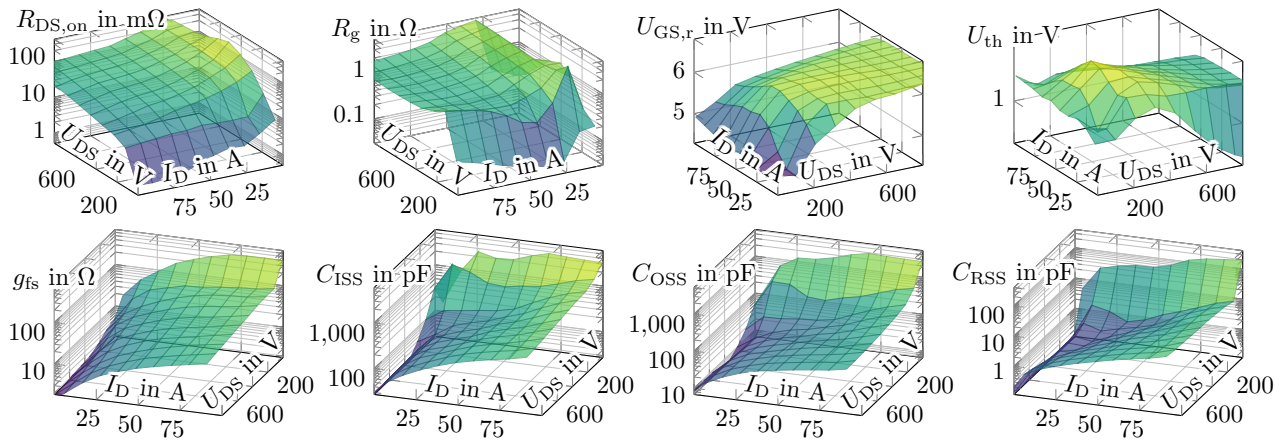


Fig. 5: Artificial GaN power transistor device parameters, predicted by the proposed machine learning model

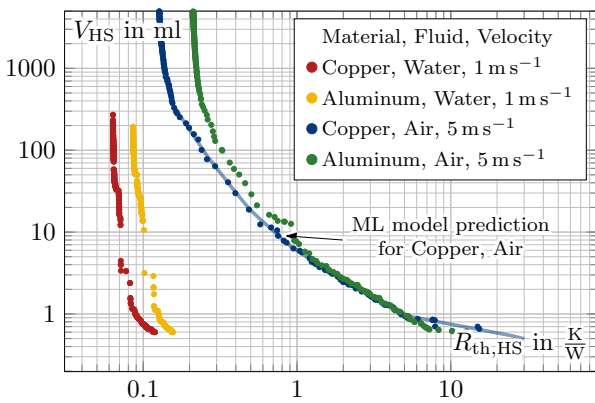


Fig. 6: Result of Pareto optimization of analytical heatsink model, ML model fit for Copper, Air trace shown

Assumptions & Constraints	Value
Thermal area of power switch	1 mm ²
$R_{th,j-c}$ of power switch	0.2 K/W
Ambient temperature T_a	30 °C
Maximum junction temperature T_j	100 °C
Length & width of base	1 cm to 20 cm
Base length-to-width ratio	< 4
Height of base	1 mm to 50 mm
Height of fin	0.1 cm to 20 cm
Width of fin	0.5 mm to 10 mm
Number of fins	2 to 500
Fin height to base dimension ratio	< 3
Fin-to-fin distance	> 1 mm

Tab. 3: Design assumptions and Pareto search constraints for heatsink precomputation

Static losses are assumed to follow Ohm’s law for the drain current and ripple current with (2).

$$P_{DC} = R_{DS,on} \left(i_{DC}^2 + \frac{i_{r,PP}^2}{12} \right) \quad (2)$$

2.2 Heatsink Design for Power Stage

The heatsink in the system context is necessary to enable sufficient heat transfer from the high loss density GaN devices to the environment. We aim to enable design with (3) given the GaN power loss P_{GaN} from section 2.1.

$$R_{th} = \frac{T_j - T_a}{P_{GaN}} - R_{th,j-c} \quad (3)$$

To obtain a heatsink volume V_{HS} from the required thermal resistance R_{th} , a description of an optimum heatsink design implementing the relation $V_{HS} = f(R_{th})$ is required. Such a custom heatsink design is itself a multi-objective

optimization problem. To retain the computation speed of our method, we precompute a Pareto optimization based on a fully analytical description of a generalized heatsink using thermodynamic approximation formulas [9, 10].

The analytical heatsink model consists of a rectangular base where heat spreads from the GaN surface area to the top of the base. Here, a variable number of vertical rectangular fins of varying sizes are attached. Both the fins and the remaining base area transfer heat by forced convection into a medium which is assumed to be at ambient temperature. We assume ideal attachment to the GaN’s $R_{th,j-c}$ without thermal interface material.

A genetic algorithm for multi-objective optimization [11] is used to find nondominant points along the Pareto front. The parameter space is constrained as given in Table 3. The resulting Pareto fronts for copper and aluminum heatsinks

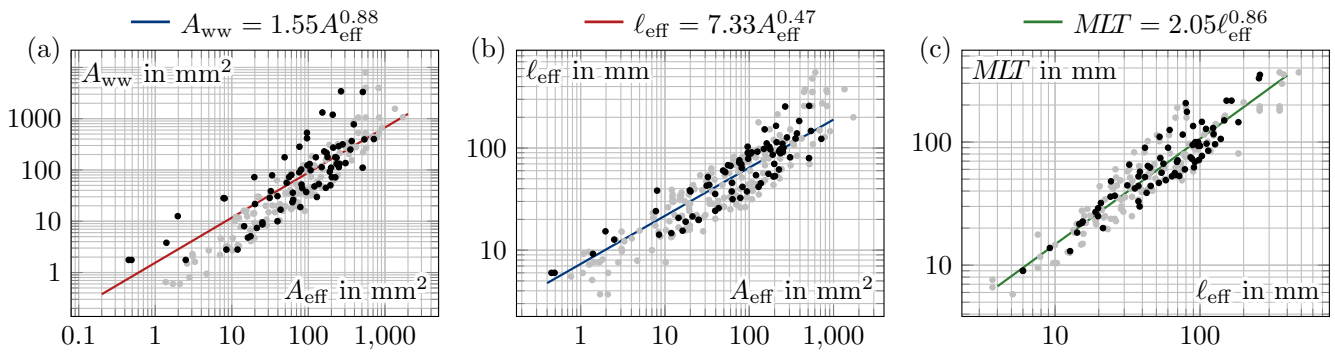


Fig. 7: Component analysis and exponential fit of magnetic core geometries, (a) winding window A_{ww} vs. effective magnetic area A_{eff} , (b) effective magnetic length l_{eff} vs. A_{eff} , (c) mean length of turn MLT vs. l_{eff}

- Ferroxcube 3C91
- Ferroxcube 3C95F
- Ferroxcube 3C97
- Ferroxcube 3F36
- Ferroxcube 3F4
- Ferroxcube 3F46
- Ferroxcube 4F1
- Magnetics L
- Magnetics R
- Magnetics T
- Magnetics W
- Magnetics Kool M μ Hf 40 μ
- Magnetics Kool M μ MAX 26 μ
- TDK N49
- TDK N95
- TDK PC200

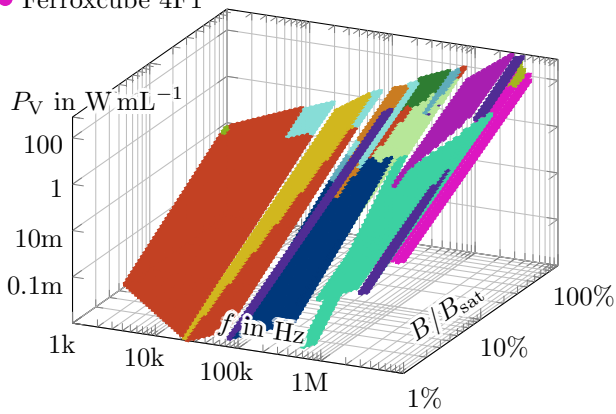


Fig. 8: Collection of lowest volumetric loss core materials, discontinuities due to operating frequencies

with air and water is shown in Fig. 6. Next, a deep neural network regressor is trained with the Pareto data, implementing the function $V_{HS} = f(R_{th})$, as this relation is not suitable for curve fitting.

2.3 Inductor Design

Inductor design is a highly active area of research, attributed to its significant number of degrees of freedom in the design space. The dependence on the geometric parameters of the magnetic core and the core material loss properties complicates design space navigation. Our approach includes three parts:

1. For the core geometry parameters (effective magnetic area A_{eff} , effective magnetic path

Assumptions	Value
Copper filling factor	0.5
Allowed inductance temperature rise	20 K
B_{max} (used in design) to B_{sat} ratio	0.8

Tab. 4: Design assumptions for inductance calculations

length l_{eff} , winding window area A_{ww} , mean length of turn MLT) we analyzed 289 core parameter sets [12, 13]. We found the relationships between these parameters to be well-defined by exponential relations, as visualized in Fig. 7. We use least-square curve fitting to extract a description for the average state-of-the-art magnetic core.

2. For the magnetic material parameters we collected volumetric material loss data from four different manufacturers for ferrite and iron power materials [12, 14–16]. Despite recent advances in the availability of inductor core loss measurement data [17] we decided to use only data provided by manufacturers to ensure greater compatibility for the near future. Each material was sampled for the volumetric loss at the same set of operating points (normalized flux density B/B_{sat} and frequency f). The data was then collected into an artificial material description containing the lowest loss of all materials for each operating point, the Steinmetz coefficients, relative permeability μ_r and saturation flux density B_{sat} . The results are presented in Fig. 8.
3. The physical inductor design is based on an area product method [13], providing all design parameters of the inductor.

Assumptions for this design process are described in Table 4.

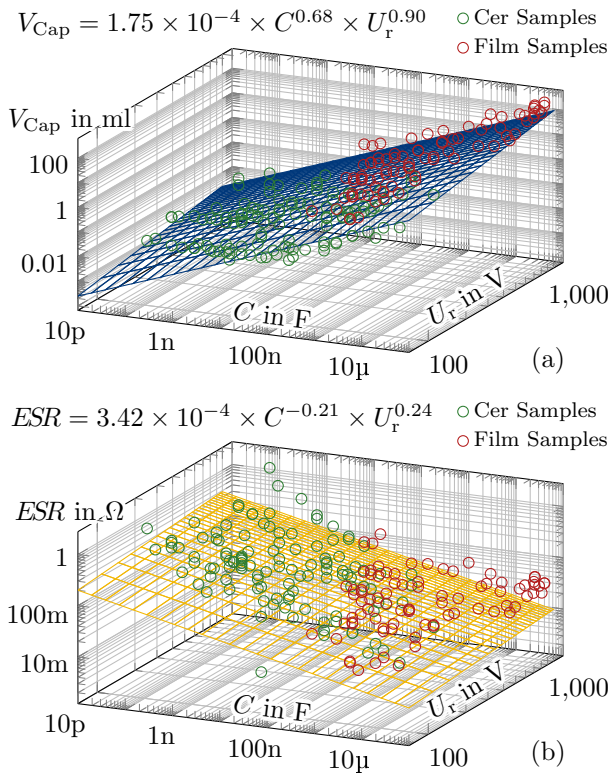


Fig. 9: Component analysis and curve fit of film and ceramic capacitors [20] for (a) volume V_{Cap} and (b) equivalent series resistance ESR

The inductance value (4) is determined by the worst-case current ripple specification to be achieved. [18]

$$L = \frac{U_{DC}}{4 \max(\langle i_r \rangle) \langle f_{sw} \rangle} \quad (4)$$

The inductor loss description includes three parts, calculated for all points in the time series voltage and current descriptions, and then averaged to obtain the total loss across one fundamental period.

1. Static losses are approximated using $\langle i_{DC} \rangle$ in Ohm's law, given the total winding resistance obtained from the design.
2. Hysteresis loss is estimated using $\langle i_r \rangle$ and $\langle f_{sw} \rangle$ in the modified Steinmetz equation [19] with the material parameters from the selected operating point of the best material (see Fig. 8).
3. Eddy current loss is estimated using $\langle i_r \rangle$ in the Dowell equation [13].

2.4 Capacitor Design

For the capacitor model we analyzed 202 multi-layer ceramic and aluminum polymer film capacitors [20]. We found that the relationships

between capacitance C , rated voltage U_r , volume V_{Cap} and equivalent series resistance ESR are well-defined by exponential relations. We employed least-square curve fitting to build two parameter sets of coefficients for the fit functions:

$$V_{Cap} = k_{V_{cap}} C^{\alpha_{V_{cap}}} U_r^{\beta_{V_{cap}}} \quad (5)$$

$$ESR = k_{ESR} C^{\alpha_{ESR}} U_r^{\beta_{ESR}} \quad (6)$$

with the coefficients shown in Fig. 9. The capacitor is dimensioned by the resulting LC low-pass filter's corner frequency

$$C = \frac{1}{4\pi^2 (\max(f_{sw}) \alpha_F)^2 L} \quad (7)$$

where $\alpha_F = 7$ according to [18]. U_r is given by the design inputs. The resulting volume is directly obtained from the fitting function. Losses caused by the ripple current $\langle i_r \rangle$ across the ESR are calculated using Ohm's law.

3 Example Applications of Design Space Exploration

The following example applications of the rapid design space exploration method demonstrate the versatility of the concept and provide insight into power electronic system dependencies. Note, that analyses with the same objective have traditionally been difficult to achieve, requiring a costly optimization routine to be run for each system configuration. Such routines typically consider many or all possible decisions along the design path, resulting in run times of hours for a single system configuration. Our implementation of the proposed method in Python on consumer-grade hardware produces several hundred system configuration analyses in less than a second. This is a significant benefit for the application engineer.

3.1 Current Ripple & Switch Frequency

In power electronics design a common tradeoff is finding the optimum switching frequency f_{sw} of a system, such that either the power loss P or the system volume V is minimized. Our method allows for the rapid generation of synthetic system configurations, each with P and V estimates, to determine the range of the optimum switching frequency f_{sw} , as visualized in Fig. 10.

This can be extended to include the current ripple as well. While our method does not model the effects of soft switching, the allowed current ripple

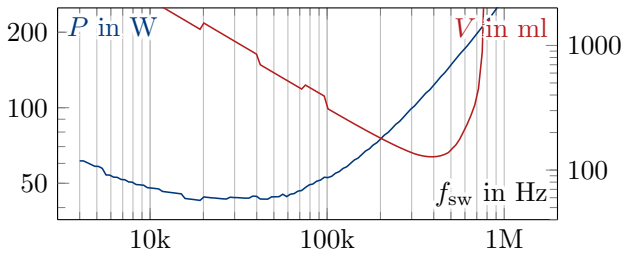


Fig. 10: Operating frequency sweep of P, V -design space for exemplary system, $U_{DC} = 400\text{ V}$, $U_{out} = 120\text{ V}_{rms}$, $P_{out} = 5\text{ kW}$, $RF = 0.12$

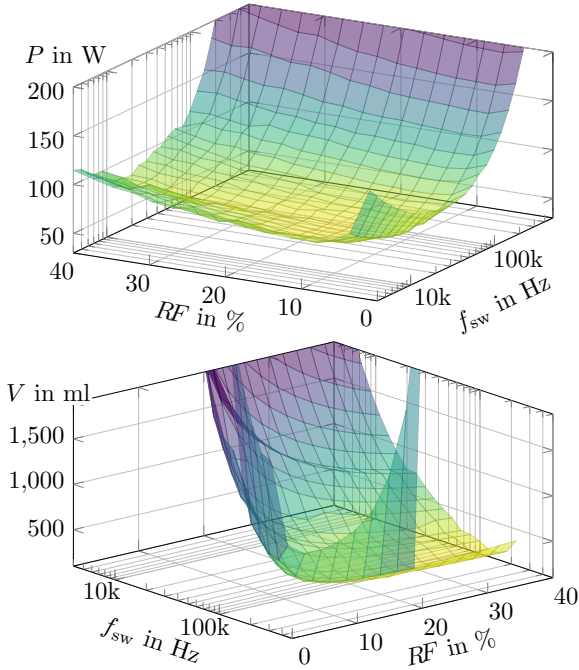


Fig. 11: Visualization of P, V -tradeoff between current ripple and switching frequency, $U_{DC} = 400\text{ V}$, $U_{out} = 120\text{ V}_{rms}$, $P_{out} = 8\text{ kW}$

factor RF can be varied alongside f_{sw} to find optimum design points in this multi-objective design space, as demonstrated in Fig. 11.

Extracting the optimum f_{sw} for different configurations of the system output power P_{out} and supply voltage U_{DC} highlights why there are different voltage classes in power electronics. Figure 12 shows that for small output powers, low voltage systems of the 48 V class feature reduced losses, while at P_{out} in the kilowatt range, high voltage systems of the 400 V class are more favorable. Since this is an expected result, it validates the approach presented in this work.

3.2 Evaluation of Modulation Techniques

Researching the influence of modulation strategy on the efficiency and power density of converters

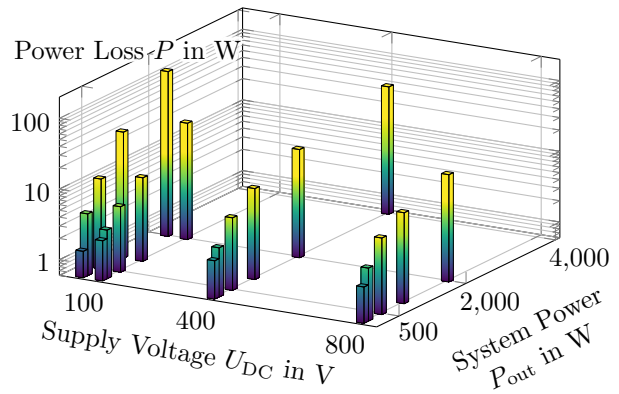


Fig. 12: Power loss P design space overview demonstrating scaling across supply voltage U_{DC} and system output power P_{out} , each system at optimum f_{sw} , $RF = 0.12$

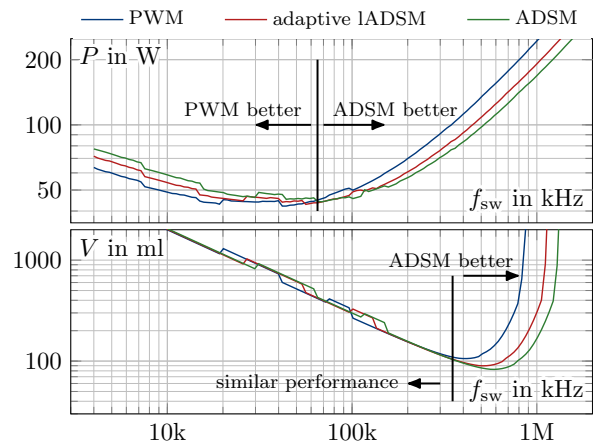


Fig. 13: Analysis of P, V -design regarding modulation strategies, showing the advantage of delta-sigma at high frequencies, $U_{DC} = 800\text{ V}$, $U_{out} = 230\text{ V}_{rms}$, $P_{out} = 4\text{ kW}$, $RF = 0.12$

is reportedly challenging [21]. As long as the influence of the modulation can be analytically expressed in terms of duty cycle and frequency, our method is applicable for a comparative analysis.

For selected system parameters we compare the influence of spread-spectrum, variable-frequency asynchronous delta-sigma modulation methods to pulse-width modulation in Fig. 13. It can be seen that delta-sigma methods achieve lower loss and lower volumes at high switching frequencies, confirming the findings from [21].

3.3 Number of Parallel and Serial Phases

We extend our system description to include the effects of interleaving parallelization and multi-level (serial) operation of the power stage. For N_{par} parallel legs, the current is

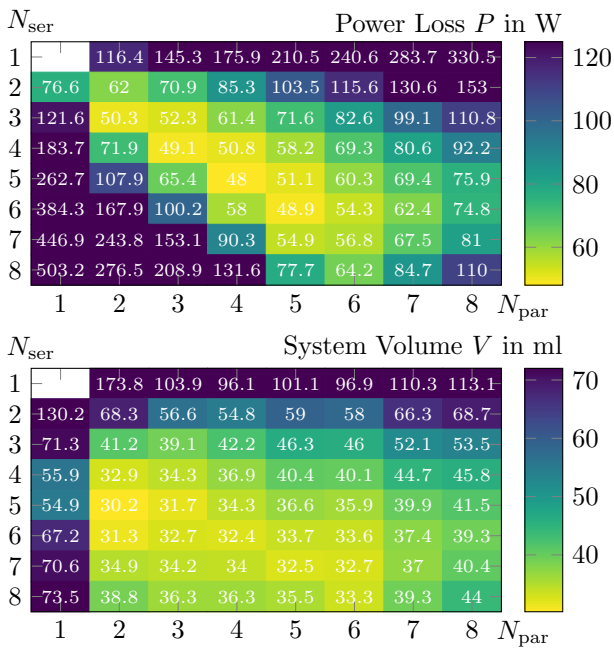


Fig. 14: Analysis of optimum number of parallel N_{par} and serial N_{ser} power stage legs in terms of power loss and system volume, with switching frequency optimized, $RF = 0.12$

reduced by $\frac{1}{N_{par}}$. For N_{ser} serial levels, the voltage differential considered for design at the inductor is reduced by $\frac{1}{N_{ser}}$. In both cases, the power stage loss and heatsink volume occur $N_{par} \times N_{ser}$ times. These simplified descriptions of multi-level and interleaving operation do not include losses in additional components necessary for parallelization or serialization. They only cover the scaling effects of such techniques, which is useful in the early stages of design for rapid prototyping.

Using our proposed exploration method, designers can generate all sensible combinations of N_{par} and N_{ser} to find the best fit for their power loss, volume, and complexity targets. Figure 14 shows the result of such an analysis for a 400 V, 12 kW system, where every system is running at its optimum frequency as described in Fig. 10. In this example the lowest loss is achieved for $N_{par} = 4, N_{ser} = 5$.

4 Conclusion

This paper presents a fast design space exploration method for GaN half-bridges with output filters, integrating analytical and machine learning techniques to efficiently generate system descriptions from performance requirements. The method includes models for the GaN-based power stage, its heatsink, and an inductor-capacitor output filter. While the method’s inherent inaccuracies

allow only approximations of the final system performance, it effectively preserves trends and scaling effects. This enables designers to uncover and analyze these aspects without the need for time-intensive simulations or optimizations, offering a versatile and efficient tool for navigating complex design spaces in power electronics.

Acknowledgment

This work was supported by the German Federal Ministry of Education and Research, FH-Kooperativ Project 13FH063KX1 "Clean Motor Supply".

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